Course Title: **Computer Programming 2**
Date: **11.06.2019 , 2nd Term(Final Exam)**

Course Code: **CCE1204** - 1st year ElectStudents
Allowed time: **3** hours – (2) pages

Answer all the following questions (Assume any missing Data):
(Note: Draw the UML diagram for all questions).

Question 1:

(18 marks)

1) Construct a **class** called **Person** has **name, age** attributes and methods: **Constructor, get, set, and display**. Then, construct another class called **Student** which ***inherits the Person class*** and has a **GPA** attribute and the same previous methods related to the student. **Write a complete C++ program which creates objects from both, the Person and Student classes. Test all the classes' methods?**

2) Construct a **class** called **Shape** has a **name** attribute and four methods: **Constructor (with default values), Get, Set, and Print**. Then, construct another class called **Circle** which ***inherits the Shape class.*** The Circle class has a **radius** attribute in addition to the same previous methods related to Circle. **Write a complete C++ program which creates objects from Circle class and print its name and radius?**

3) **Implement a class Point that has the following characteristics:**
   a) **Constructors** including a default constructor that sets the Point to the origin.
   b) **Modifier methods** to modify the coordinate of the point.
   c) **Access methods** to know the point coordinates.
   d) A method **Move**: that shift the coordinate of the point.
   e) A method to **display** the coordinate of the Point.

   Write a C++ program to test your class by creating an object from Point class with values (4, 2). Print its value and then Move this point to the location (5, 7).

Question 2:

(18 marks)

1) Construct a **class** called **Animal** has **Name and Age** attributes and three methods: **Constructor (with memory allocation for the Name attribute), Set, and display**. Then, construct another class called **Cat** which ***inherits the Animal class*** and has a **NumOfLegs** attribute and the same previous methods related to the animal. **Write a complete C++ program which creates an object from the Cat class and display its all information?**
2) Construct a **class** called **Employee** has **name, ID, workhours** attributes and methods: **Constructor, get, set, and display**. Then, construct another class called **Engineer** that inherits the Employee class and it has a **Salary** attribute and the same previous methods related to the Employee.
   Write a complete C++ program that creates objects from both, the Employee and Engineer classes. Test all the classes' methods? (Draw the UML diagram).

3) Create a **structure** data type called **Cylinder**. The structure has two Members: **radius**, and **thickness**. Provide the following functions:
   a) **Area ( )** to calculate the side area of a Cylinder.
   b) **Circumference ( )** to calculate the perimeter of a Cylinder section.
   c) **Volume ( )** to calculate the volume of a Cylinder.
   d) **Printing** circle members in the form (A, C, V) where A is the side Area, C is Circumference of the base, and V is the volume of a Cylinder respectively.

Write a C++ program to test your structure and functions.

Question 3:

(24 marks)

1) Create a **structure data type** called **Complex** for performing arithmetic with complex numbers. Provide the following functions:
   a. **Addition** of two complex numbers.
   b. **Subtraction** of two complex numbers.
   c. **Multiplication** of two complex numbers.
   d. **Printing** complex members in the form **(R,IM)** where **R is the real part and IM is the imaginary part.**

Write a C++ program to test your structure and functions.

2) Create a **structure** data type called **GPAStudent** for entering marks of 10 subjects (use conversional method). The data are **studID**, **subjName**, **subjMark**. The data will be stored in a table then calculate the **totalGPA** of the subjects. Display the output including all data, and **totalGPA**.

Write a C++ program to test your structure and functions.

3) It is required to design and implement an **array class**, called **Database**. The class should provide the following features:
   a) **A constructor that creates a dynamic store** for the elements in **an array. The default constructor should store up to 100 items of integers.**
   b) **A destructor.**
   c) **A method, Find( ), that can check if a given item is in the array or not.**
   d) **A method, Insert( ), that can insert a given item into the array.**
   e) **A method, Delete( ), that can delete a given element from the array.**
   f) **A method, Display( ), that can display the contents of the array.**

An object of **Database** contains an array of integers with the following values **(88, 33, 22, 66, 00, 77, 22, 99, 11, 44)** stored by the **Insert** Function. The program would also ask its user (conversional, alert) to enter an item from the keyboard that to be deleted from the array. The object should response to the user by display the current elements in the array. **Finally, write a complete C++ program that can accomplish all of the above tasks. (Draw the UML diagram).**

With best wishes,

Prof. Dr. Elsayed Sallam

11. An example of a replacement algorithm is
(a) LED
(b) LRU
(c) LDR
(d) LNT

12. Consider a virtual memory system that can address a total of 2^{50} bytes. You have unlimited hard drive space, but are limited to 2 GB of semiconductor (physical) memory. Assume that virtual and physical pages are each 4 KB in size. What is the maximum number of virtual pages in the system?
(a) 31 bits
(b) 38 bits
(c) 19 bits
(d) None of These

13. A memory system uses the Least Recently Used (LRU) replacement policy for a 4-block cache. If the following sequence of blocks was requested, A B C D E F D A C D, what are the blocks that eventually found in chache
(a) F, D, A, C
(b) D, A, C, D
(c) E, F, A, C
(d) E, F, A, D

14. Addressing modes define where . . . . . are located in.
(a) Operations
(b) Instructions
(c) Operands
(d) None of these

15. In direct addressing mode the operand is given. . . . . in the instruction.
(a) Implicit
(b) Explicit
(c) Not Given
(d) None of these

Questions 16 to 18: A computer system uses 32-bit memory addresses. It has a 128K-byte 8-way set-associative (8 blocks per set) cache, with 64 bytes per cache block. Assume that the size of each memory word is **1** byte.
16. The number of bits in each of the Tag, Set, and Word fields of the memory address
(a) 11, 8, and 6 respectively
(b) 18, 8, and 6 respectively
(c) 15, 9, and 6 respectively
(d) 20, 6, and 8 respectively

17. If direct mapping is used, the number of bits in each of Tag, block, and Word fields of the memory address
(a) 18, 8, and 6 respectively
(b) 15, 8, and 7 respectively
(c) 15, 9, and 6 respectively
(d) 24, 9, and 6 respectively

18. If fully associative mapping is used, the number of bits in each of Tag and Word fields of the memory address
(a) 26 and 6 respectively
(b) 11 and 6 respectively
(c) 32 and 6 respectively
(d) 32 and 0 respectively

19. Consider a 128 M x 128 memory. How many address bits are needed to access the memory?
(a) 23
(b) 30
(c) 40
(d) 27

20. When using virtual memory, information about the main memory location of each page is kept in a.....
(a) register file.
(b) hard disk.
(c) page table.
(d) ROM.

21. The memory address register (MAR) is
(a) A general purpose register that hold operands of instructions
(b) A stack pointer
(c) A special registers points to (holds the address of) the memory location that will be read or written to
(d) A register that holds the instruction that is being executed

22. Memory chip external connections, in which a line is connected to every bit in the selected location for i/o.
(a) data lines.
(b) address lines.
(c) control lines.
(d) power lines.

Answer the following questions

Question 1(34 pts): Choose the correct answer

1. What is the type of the following MIPS instruction which has 0x02328020 Machine code.
(a) I-Type
(b) J-Type
(c) R-Type
(d) None of these

2. The control unit (CU) in the processor is responsible for
(a) Addition
(b) Comparison of numbers
(c) Multiplication
(d) Timing signals

3. A processor with 26 address bits supports memory up to
(a) 128K word
(b) 32K word
(c) 64K word
(d) 64M word

4. Suppose t0 initially contains 0x23456789, After following code runs on big-endian system, what value is $s0?
sw $t0, 0($0)
lb $s0, 1($0)
(a) 0x00000023
(b) 0x00000045
(c) 0x00000089
(d) 0x00000067

5. RAM is called DRAM (Dynamic RAM) when
(a) it is always moving around data
(b) it requires periodic refreshing
(c) it can do several things simultaneously
(d) None of these

6. In the instruction Load R5, (R4), the (R4) is an example of the addressing mode
(a) Absolute
(b) Register Indirect
(c) Index.
(d) Base with Index

7. Convert the following MIPS assembly code into machine language *sub$t1, $s7, $s2*
(a) 00010000000100001111001111110110
(b) 00010000000100001101111111110110
(c) 00010001100100001111111111110110
(d) 00000010111100100100100000100010

8. A Direct mapped cache has a capacity of 16-word cache and a block size of 1 word. Consider the following repeating sequence of lw addresses (given in hexadecimal): 74 A0 78 38C AC 84 88 8C 7C 34 38 13C 388 18C Determine the effective miss rate if the sequence is input to the following caches, ignoring start up effects.
(a) 100%
(b) 70%
(c) 50%
(d) 20%

9. Which MIPS-32 addressing mode allows you to specify a constant in the instruction that can be directly used by the CPU without needing any data from the registers or memory?
(a) Register-only addressing
(b) PC-Relative Addressing
(c) Immediate addressing
(d) All of the above

10. The program counter (PC) is a special register that
(a) holds the instruction that is currently being executed.
(b) is a pointer to the top of the stack.
(c) contains the memory address of the next instruction to be fetched and executed.
(d) Holds an operand of an arithmetic operation.

23. Dynamic RAM cells are implemented as
(a) CMOS.
(b) capacitor.
(c) inverters.
(d) Magnetized material

24. After executing the following assembly instruction: Load R4, (R5) register R4 contains
(a) The same value stored in R5
(b) Zero
(c) The same value stored in the memory location that R5 points to
(d) An arbitrary value that was stored by another program earlier.

25. What is the machine code for *addi $s0,$0,73*
(a) 0X018D4044
(b) 0X01654024
(c) 0x20100049
(d) 0X016D40F9

26. A 128M x 8 memory system is being constructed by using 16M x 8 memory chips. How many chips are needed?
(a) 8
(b) 32
(c) 64
(d) None of these

27. If multiplexers are used to construct a common bus system for 6 registers of 32 bit each. How many MUX do you need?
(a) twenty
(b) six
(c) thirty two
(d) none is correct

28. A Fully associative cache has a capacity of 16-word cache and a block size of 2 words. Consider the following repeating sequence of lw addresses (given in hexadecimal): 74 A0 78 38C AC 84 88 8C 7C 34 38 13C 388 18C..Assuming least recently used (LRU) replacement for associative caches, determine the effective miss rate if the sequence is input to the following caches, ignoring startup effects.
(a) 30%
(b) 70%
(c) 50%
(d) None of these

29. MIPS-32 has.....word size
(a) 16-bit
(b) 32-bit
(c) 64-bit
(d) None of These

30. A recently executed instruction is likely to be executed again very soon is
(a) spatial locality.
(b) temporal locality.
(c) branch prediction.
(d) compiler optimization.

31. The cache memory is faster than
(a) Hard disk
(b) Main memory
(c) CD/DVD.
(d) All of the above

32. The main memory is slower than
(a) Hard disk
(b) CD
(c) virtual memory
(d) Cache memory

33. Suppose processor has 2 levels of hierarchy: cache and main memory tcache = 1 cycle, tMM = 100 cycles, MRcache=0.625, What is the AMAT of the program?
(a) 63.5 cycles
(b) 40 cycles
(c) 20 cycles
(d) 15 cycles

34. A processor uses 44-bit virtual addresses with 4 KB pages. Which bits in the virtual address correspond to the "virtual page number" field?
(a) The most significant 34 bits
(b) The least significant 32 bits
(c) The most significant 32 bits
(d) The least significant 12 bits

Question 2 (6 pts): True or False

1. A page table acts as a cache for the Translation Lookaside Buffer (TLB).

2. A write-through cache need a "dirty" bit for each cache line.

3. A write-back cache typically requires more reads to the main memory than a write-through cache.

4. The main purpose of using larger cache block sizes is to reduce the cache access time.

5. SRAM is more expensive on a cost-per-bit basis as compared to DRAM.

6. A "word" is the natural unit of organization of memory. Different computers may have different word lengths (in bits).

Question 3 (30 pts)

1) Define each of the following:**[04 Marks]**
(i)Cache, ***(ii)*** Virtual Memory, ***(iii)***Hit Rate, ***(iv)*** Miss Rate

2) Show the main difference between temporal and spatial locality? **[02 Marks]**

3) Program to calculate Absolute value of difference between **[10 Marks]**
2 input numbers: |A - B| where:
Program reads A from 4 bytes of memory starting at address 12345670_{16}.
Program reads B from 4 bytes of memory starting at address 12345674_{16}.
Program writes |A-B| to4 bytes of memory starting at address 12345678_{16}.

4) Implement the following C code with MIPS assembly language. **[14 Marks]**

```
// C code
void setArray(int num) {
int i;
int array[10];
for (i = 0; i < 10; i = i + 1) {
array[i] = compare(num, i);
}
}
int compare(int a, int b) {
if (sub(a, b) >= 0)
return 1;
else
return 0;
}
int sub(int a, int b) {
return a – b;
}
```

Mnemonics	Code
Add	32
Sub	34
Addi	8
$s0	16
$s1	17
$s2	18
$s7	23
$t0	8
$t1	9
$t3	11
$t5	13

Good Luck all,
Dr. Nada M. Elshennawy

(b) 32
(c) 64
(d) None of these

11. The cache memory is faster than
(a) Hard disk
(b) Main memory
(c) CD/DVD.
(d) All of the above

12. Dynamic RAM cells are implemented as
(a) CMOS.
(b) capacitor.
(c) inverters.
(d) Magnetized material

13. An example of a replacement algorithm is
(a) LED
(b) LRU
(c) LDR
(d) LNT

14. Suppose processor has 2 levels of hierarchy: cache and main memory tcache = 1 cycle, tMM = 100 cycles, MRcache=0.625, What is the AMAT of the program?
(a) 63.5 cycles
(b) 40 cycles
(c) 20 cycles
(d) 15 cycles

15. Convert the following MIPS assembly code into machine language *sub$t1, $s7, $s2*
(a) 00010000000100001111001111110110
(b) 00010000000100001101111111110110
(c) 00010001100100001111111111110110
(d) 00000010111100100100100000100010

16. Memory chip external connections, in which a line is connected to every bit in the selected location for i/o.
(a) data lines.
(b) address lines.
(c) control lines.
(d) power lines.

17. RAM is called DRAM (Dynamic RAM) when
(a) it is always moving around data
(b) it requires periodic refreshing
(c) it can do several things simultaneously
(d) None of these

18. In direct addressing mode the operand is given. . . . . in the instruction.
(a) Implicit
(b) Explicit
(c) Not Given
(d) None of these

19. The control unit (CU) in the processor is responsible for
(a) Addition
(b) Comparison of numbers
(c) Multiplication
(d) Timing signals

20. The main memory is slower than
(a) Hard disk
(b) CD
(c) virtual memory
(d) Cache memory

21. Suppose t0 initially contains 0x23456789, After following code runs on big-endian system, what value is $s0?
sw $t0, 0($0)
lb $s0, 1($0)
(a) 0x00000023
(b) 0x00000045
(c) 0x00000089
(d) 0x00000067

22. A Direct mapped cache has a capacity of 16-word cache and a block size of 1 word. Consider the following repeating sequence of lw addresses (given in hexadecimal): 74 A0 78 38C AC 84 88 8C 7C 34 38 13C 388 18C Determine the effective miss rate if the sequence is input to the following caches, ignoring start up effects.
(a) 100%
(b) 70%
(c) 50%
(d) 20%

23. A memory system uses the Least Recently Used (LRU) replacement policy for a 4-block cache. If the following sequence of blocks was requested, A B C D E F D A C D, what are the blocks that eventually found in chache
(a) F, D, A, C
(b) D, A, C, D
(c) E, F, A, C

Course Title: Computer Hardware		Course Code: CCE1205	Year: 1st
Date: June 13rd 2019	**Model C**	Allowed time: 3 hrs	No. of Pages: (4)

Answer the following questions

Question 1(34 pts): Choose the correct answer

1. In the instruction Load R5, (R4), the (R4) is an example of the addressing mode
(a) Absolute
(b) Register Indirect
(c) Index.
(d) Base with Index

2. What is the machine code for *addi $s0,$0,73*
(a) 0X018D4044
(b) 0X01654024
(c) 0x20100049
(d) 0X016D40F9

3. After executing the following assembly instruction: Load R4, (R5) register R4 contains
(a) The same value stored in R5
(b) Zero
(c) The same value stored in the memory location that R5 points to
(d) An arbitrary value that was stored by another program earlier.

4. Addressing modes define where . . . . . are located in.
(a) Operations
(b) Instructions
(c) Operands
(d) None of these

5. A Fully associative cache has a capacity of 16-word cache and a block size of 2 words. Consider the following repeating sequence of lw addresses (given in hexadecimal): 74 A0 78 38C AC 84 88 8C 7C 34 38 13C 388 18C..Assuming least recently used (LRU) replacement for associative caches, determine the effective miss rate if the sequence is input to the following caches, ignoring startup effects.
(a) 30%
(b) 70%
(c) 50%
(d) None of these

6. Consider a virtual memory system that can address a total of 2^{50} bytes. You have unlimited hard drive space, but are limited to 2 GB of semiconductor (physical) memory. Assume that virtual and physical pages are each 4 KB in size. What is the maximum number of virtual pages in the system?
(a) 31 bits
(b) 38 bits
(c) 19 bits
(d) None of These

7. Which MIPS-32 addressing mode allows you to specify a constant in the instruction that can be directly used by the CPU without needing any data from the registers or memory?
(a) Register-only addressing
(b) PC-Relative Addressing
(c) Immediate addressing
(d) All of the above

8. MIPS-32 has.....word size
(a) 16-bit
(b) 32-bit
(c) 64-bit
(d) None of These

9. When using virtual memory, information about the main memory location of each page is kept in a.....
(a) register file.
(b) hard disk.
(c) page table.
(d) ROM.

10. A 128M x 8 memory system is being constructed by using 16M x 8 memory chips. How many chips are needed?
(a) 8

(d) E, F, A, D

24. A recently executed instruction is likely to be executed again very soon is
(a) spatial locality.
(b) temporal locality.
(c) branch prediction.
(d) compiler optimization.

Questions 25 to 27: A computer system uses 32-bit memory addresses. It has a 128K-byte 8-way set-associative (8 blocks per set) cache, with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.

25. The number of bits in each of the Tag, Set, and Word fields of the memory address
(a) 11, 8, and 6 respectively
(b) 18, 8, and 6 respectively
(c) 15, 9, and 6 respectively
(d) 20, 6, and 8 respectively

26. If direct mapping is used, the number of bits in each of Tag, block, and Word fields of the memory address
(a) 18, 8, and 6 respectively
(b) 15, 8, and 7 respectively
(c) 15, 9, and 6 respectively
(d) 24, 9, and 6 respectively

27. If fully associative mapping is used, the number of bits in each of Tag and Word fields of the memory address
(a) 26 and 6 respectively
(b) 11 and 6 respectively
(c) 32 and 6 respectively
(d) 32 and 0 respectively

28. What is the type of the following MIPS instruction which has 0x02328020 Machine code.
(a) I-Type
(b) J-Type
(c) R-Type
(d) None of these

29. The program counter (PC) is a special register that
(a) holds the instruction that is currently being executed.
(b) is a pointer to the top of the stack.
(c) contains the memory address of the next instruction to be fetched and executed.
(d) Holds an operand of an arithmetic operation.

30. Consider a 128 M x 128 memory. How many address bits are needed to access the memory?
(a) 23
(b) 30
(c) 40
(d) 27

31. The memory address register (MAR) is
(a) A general purpose register that hold operands of instructions
(b) A stack pointer
(c) A special registers points to (holds the address of) the memory location that will be read or written to
(d) A register that holds the instruction that is being executed

32. A processor with 26 address bits supports memory up to
(a) 128K word
(b) 32K word
(c) 64K word
(d) 64M word

33. If multiplexers are used to construct a common bus system for 6 registers of 32 bit each. How many MUX do you need?
(a) twenty
(b) six
(c) thirty two
(d) none is correct

34. A processor uses 44-bit virtual addresses with 4 KB pages. Which bits in the virtual address correspond to the "virtual page number" field?
(a) The most significant 34 bits
(b) The least significant 32 bits
(c) The most significant 32 bits
(d) The least significant 12 bits

Question 2 (6 pts): True or False

1. A page table acts as a cache for the Translation Lookaside Buffer (TLB).

2. A write-through cache need a "dirty" bit for each cache line.

3. A write-back cache typically requires more reads to the main memory than a write-through cache.

4. The main purpose of using larger cache block sizes is to reduce the cache access time.

5. SRAM is more expensive on a cost-per-bit basis as compared to DRAM.

6. A "word" is the natural unit of organization of memory. Different computers may have different word lengths (in bits).

Question 3 (30 pts)

1) Define each of the following:**[04 Marks]**
(i)Cache, ***(ii)*** Virtual Memory, ***(iii)***Hit Rate, ***(iv)*** Miss Rate
2) Show the main difference between temporal and spatial locality? **[02 Marks]**

3) Program to calculate Absolute value of difference between **[10 Marks]**
2 input numbers: |A - B| where:
Program reads A from 4 bytes of memory starting at address 12345670_{16}.
Program reads B from 4 bytes of memory starting at address 12345674_{16}.
Program writes |A-B| to4 bytes of memory starting at address 12345678_{16}.

4) Implement the following C code with MIPS assembly language. **[14 Marks]**

```
// C code
void setArray(int num) {
int i;
int array[10];
for (i = 0; i < 10; i = i + 1) {
array[i] = compare(num, i);
}
}
int compare(int a, int b) {
if (sub(a, b) >= 0)
return 1;
else
return 0;
}
int sub(int a, int b) {
return a − b;
}
```

Mnemonics	Code
Add	32
Sub	34
Addi	8
$s0	16
$s1	17
$s2	18
$s7	23
$t0	8
$t1	9
$t3	11
$t5	13

Good Luck all,
Dr. Nada M. Elshennawy

Answer the following questions

Question 1(34 pts): Choose the correct answer

1. If multiplexers are used to construct a common bus system for 6 registers of 32 bit each. How many MUX do you need?
(a) twenty
(b) six
(c) thirty two
(d) none is correct

2. What is the type of the following MIPS instruction which has 0x02328020 Machine code.
(a) I-Type
(b) J-Type
(c) R-Type
(d) None of these

3. Dynamic RAM cells are implemented as
(a) CMOS.
(b) capacitor.
(c) inverters.
(d) Magnetized material

4. The cache memory is faster than
(a) Hard disk
(b) Main memory
(c) CD/DVD.
(d) All of the above

5. The main memory is slower than
(a) Hard disk
(b) CD
(c) virtual memory
(d) Cache memory

6. Which MIPS-32 addressing mode allows you to specify a constant in the instruction that can be directly used by the CPU without needing any data from the registers or memory?
(a) Register-only addressing
(b) PC-Relative Addressing
(c) Immediate addressing
(d) All of the above

7. A Direct mapped cache has a capacity of 16-word cache and a block size of 1 word. Consider the following repeating sequence of lw addresses (given in hexadecimal): 74 A0 78 38C AC 84 88 8C 7C 34 38 13C 388 18C Determine the effective miss rate if the sequence is input to the following caches, ignoring start up effects.
(a) 100%
(b) 70%
(c) 50%
(d) 20%

8. What is the machine code for *addi $s0,$0,73*
(a) 0X018D4044
(b) 0X01654024
(c) 0X20100049
(d) 0X016D40F9

9. A 128M x 8 memory system is being constructed by using 16M x 8 memory chips. How many chips are needed?
(a) 8
(b) 32
(c) 64
(d) None of These

10. Convert the following MIPS assembly code into machine language sub$t1, $s7, $s2
(a) 00010000000100001111001111110110
(b) 00010000000100001101111111110110
(c) 00010001100100001111111111110110
(d) 00000010111100100100100000100010

11. Consider a 128 M x 128 memory. How many address bits are needed to access the memory?
(a) 23
(b) 30
(c) 40
(d) 27

12. MIPS-32 has.....word size
(a) 16-bit
(b) 32-bit
(c) 64-bit
(d) None of These

13. A recently executed instruction is likely to be executed again very soon is
(a) spatial locality.
(b) temporal locality.
(c) branch prediction.
(d) compiler optimization.

14. When using virtual memory, information about the main memory location of each page is kept in a .....
(a) register file.
(b) hard disk.
(c) page table.
(d) ROM.

15. Consider a virtual memory system that can address a total of 2^{50} bytes. You have unlimited hard drive space, but are limited to 2 GB of semiconductor (physical) memory. Assume that virtual and physical pages are each 4 KB in size. What is the maximum number of virtual pages in the system?
(a) 31 bits
(b) 38 bits
(c) 19 bits
(d) None of These

16. RAM is called DRAM (Dynamic RAM) when
(a) it is always moving around data
(b) it requires periodic refreshing
(c) it can do several things simultaneously
(d) None of these

17. Suppose $t0 initially contains 0x23456789, After following code runs on big-endian system, what value is $s0?
sw $t0, 0($0)
lb $s0, 1($0)
(a) 0x00000023
(b) 0x00000045
(c) 0x00000089
(d) 0x00000067

18. The program counter (PC) is a special register that
(a) holds the instruction that is currently being executed.
(b) is a pointer to the top of the stack.
(c) contains the memory address of the next instruction to be fetched and executed.
(d) Holds an operand of an arithmetic operation.

19. The memory address register (MAR) is
(a) A general purpose register that hold operandsof instructions
(b) A stack pointer
(c) A special registers points to (holds the address of) the memory location that will be read or written to
(d) A register that holds the instruction that is being executed

20. After executing the following assembly instruction: Load R4, (R5) register R4 contains
(a) The same value stored in R5
(b) Zero
(c) The same value stored in the memory location that R5 points to
(d) An arbitrary value that was stored by another program earlier.

21. An example of a replacement algorithm is
(a) LED
(b) LRU
(c) LDR
(d) LNT

22. A Fully associative cache has a capacity of 16-word cache and a block size of 2 words. Consider the following repeating sequence of lw addresses (given in hexadecimal): 74 A0 78 38C AC 84 88 8C 7C 34 38 13C 388 18C..Assuming least recently used (LRU) replacement for associative caches, determine the effective miss rate if the sequence is input to the following caches, ignoring startup effects.
(a) 30%
(b) 70%
(c) 50%
(d) None of these

23. A memory system uses the Least Recently Used (LRU) replacement policy for a 4-block cache. If the following sequence of blocks

was requested, A B C D E F D A C D, what are the blocks that eventually found in chache
(a) F, D, A, C
(b) D, A, C, D
(c) E, F, A, C
(d) E, F, A, D

24. A processor with 26 address bits supports memory up to
(a) 128K word
(b) 32K word
(c) 64K word
(d) 64M word

25. The control unit (CU) in the processor is responsible for
(a) Addition
(b) Comparison of numbers
(c) Multiplication
(d) Timing signals

Questions 26 to 28: A computer system uses 32-bit memory addresses. It has a 128K-byte 8-way set-associative (8 blocks per set) cache, with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.
26. The number of bits in each of the Tag, Set, and Word fields of the memory address
(a) 11, 8, and 6 respectively
(b) 18, 8, and 6 respectively
(c) 15, 9, and 6 respectively
(d) 20, 6, and 8 respectively

27. If direct mapping is used, the number of bits in each of Tag, block, and Word fields of the memory address
(a) 18, 8, and 6 respectively
(b) 15, 8, and 7 respectively
(c) 15, 9, and 6 respectively
(d) 24, 9, and 6 respectively

28. If fully associative mapping is used, the number of bits in each of Tag and Word fields of the memory address
(a) 26 and 6 respectively
(b) 11 and 6 respectively
(c) 32 and 6 respectively
(d) 32 and 0 respectively

29. A processor uses 44-bit virtual addresses with 4 KB pages. Which bits in the virtual address correspond to the "virtual page number" field?
(a) The most significant 34 bits
(b) The least significant 32 bits
(c) The most significant 32 bits
(d) The least significant 12 bits

30. Memory chip external connections, in which a line is connected to every bit in the selected location for i/o.
(a) data lines.
(b) address lines.
(c) control lines.
(d) power lines

31. Suppose processor has 2 levels of hierarchy: cache and main memory tcache = 1 cycle, tMM = 100 cycles, MRcache=0.625, What is the AMAT of the program?
(a) 63.5 cycles
(b) 40 cycles
(c) 20 cycles
(d) 15 cycles

32. In direct addressing mode the operand is given. . . . . in the instruction.
(a) Implicit
(b) Explicit
(c) Not Given
(d) None of these

33. In the instruction Load R5, (R4), the (R4) is an example of the addressing mode
(a) Absolute
(b) Register Indirect
(c) Index.
(d) Base with Index

34. Addressing modes define where . . . . . are located in.
(a) Operations
(b) Instructions
(c) Operands
(d) None of these

Question 2 (6 pts): True or False

1. A page table acts as a cache for the Translation Lookaside Buffer (TLB).

2. A write-through cache need a "dirty" bit for each cache line.

3. A write-back cache typically requires more reads to the main memory than a write-through cache.

4. The main purpose of using larger cache block sizes is to reduce the cache access time.

5. SRAM is more expensive on a cost-per-bit basis as compared to DRAM.

6. A "word" is the natural unit of organization of memory. Different computers may have different word lengths (in bits).

Question 3 (30 pts)

1) Define each of the following:**[04 Marks]**
(i)Cache, ***(ii)*** Virtual Memory, ***(iii)***Hit Rate, ***(iv)*** Miss Rate

2) Show the main difference between temporal and spatial locality? **[02 Marks]**

3) Program to calculate Absolute value of difference between **[10 Marks]**
2 input numbers: |A - B| where:
Program reads A from 4 bytes of memory starting at address 12345670_{16}.
Program reads B from 4 bytes of memory starting at address 12345674_{16}.
Program writes |A-B| to4 bytes of memory starting at address 12345678_{16}.

4) Implement the following C code with MIPS assembly language. **[14 Marks]**

```
// C code
void setArray(int num) {
int i;
int array[10];
for (i = 0; i < 10; i = i + 1) {
array[i] = compare(num, i);
}
}
int compare(int a, int b) {
if (sub(a, b) >= 0)
return 1;
else
return 0;
}
int sub(int a, int b) {
return a − b;
}
```

Mnemonics	Code
Add	32
Sub	34
Addi	8
$s0	16
$s1	17
$s2	18
$s7	23
$t0	8
$t1	9
$t3	11
$t5	13

Good Luck all,
Dr. Nada M. Elshennawy

Tanta University — Department: Computers and Automatic Control Eng. — Faculty of Engineering

Total Marks: 70 Marks

Course Title: Computer Hardware		Course Code: CCE1205	Year: 1st
Date: June 13rd 2019	**Model A**	Allowed time: 3 hrs	No. of Pages: (4)

Answer the following questions

Question 1(34 pts): Choose the correct answer

1.Suppose t0 initially contains 0x23456789, After following code runs on big-endian system, what value is s0?
sw $t0, 0($0)
lb $s0, 1($0)
(a) 0x00000023
(b) 0x00000045
(c) 0x00000089
(d) 0x00000067

2. The main memory is slower than
(a) Hard disk
(b) CD
(c) virtual memory
(d) Cache memory

3. Dynamic RAM cells are implemented as
(a) CMOS.
(b) capacitor.
(c) inverters.
(d) Magnetized material

4. After executing the following assembly instruction: Load R4, (R5) register R4 contains
(a) The same value stored in R5
(b) Zero
(c) The same value stored in the memory location that R5 points to
(d) An arbitrary value that was stored by another program earlier.

5. An example of a replacement algorithm is
(a) LED
(b) LRU
(c) LDR
(d) LNT

6. When using virtual memory, information about the main memory location of each page is kept in a .....
(a) register file.
(b) hard disk.
(c) page table.
(d) ROM.

7. RAM is called DRAM (Dynamic RAM) when
(a) it is always moving around data
(b) it requires periodic refreshing
(c) it can do several things simultaneously
(d) None of these

8. A Direct mapped cache has a capacity of 16-word cache and a block size of 1 word. Consider the following repeating sequence of lw addresses (given in hexadecimal): 74 A0 78 38C AC 84 88 8C 7C 34 38 13C 388 18C Determine the effective miss rate if the sequence is input to the following caches, ignoring start up effects.
(a) 100%
(b) 70%
(c) 50%
(d) 20%

9. What is the machine code for *addi $s0,$0,73*
(a) 0X018D4044
(b) 0X01654024
(c) 0x20100049
(d) 0X016D40F9

10. The control unit (CU) in the processor is responsible for
(a) Addition
(b) Comparison of numbers
(c) Multiplication
(d) Timing signals

11. A processor with 26 address bits supports memory up to
(a) 128K word
(b) 32K word
(c) 64K word
(d) 64M word

12. Memory chip external connections, in which a line is connected to every bit in the selected location for i/o.
(a) data lines.
(b) address lines.
(c) control lines.
(d) power lines.

13. A 128M x 8 memory system is being constructed by using 16M x 8 memory chips. How many chips are needed?
(a) 8
(b) 32
(c) 64
(d) None of these

14. Suppose processor has 2 levels of hierarchy: cache and main memory tcache = 1 cycle, tMM = 100 cycles, MRcache=0.625, What is the AMAT of the program?
(a) 63.5 cycles
(b) 40 cycles
(c) 20 cycles
(d) 15 cycles

15. In the instruction Load R5, (R4), the (R4) is an example of the addressing mode
(a) Absolute
(b) Register Indirect
(c) Index.
(d) Base with Index

16. A Fully associative cache has a capacity of 16-word cache and a block size of 2 words. Consider the following repeating sequence of lw addresses (given in hexadecimal): 74 A0 78 38C AC 84 88 8C 7C 34 38 13C 388 18C..Assuming least recently used (LRU) replacement for associative caches, determine the effective miss rateif the sequence is input to the following caches, ignoring startup effects.
(a) 30%
(b) 70%
(c) 50%
(d) None of these

17. What is the type of the following MIPS instruction which has 0x02328020 Machine code.
(a) I-Type
(b) J-Type
(c) R-Type
(d) None of these

18. The program counter (PC) is a special register that
(a) holds the instruction that is currently being executed.
(b) is a pointer to the top of the stack.
(c) contains the memory address of the next instruction to be fetched and executed.
(d) Holds an operand of an arithmetic operation.

19. Which MIPS-32 addressing mode allows you to specify a constant in the instruction that can be directly used by the CPU without needing any data from the registers or memory?
(a) Register-only addressing
(b) PC-Relative Addressing
(c) Immediate addressing
(d) All of the above

20. Addressing modes define where . . . . . are located in.
(a) Operations
(b) Instructions
(c) Operands
(d) None of these

21. The cache memory is faster than
(a) Hard disk
(b) Main memory
(c) CD/DVD.
(d) All of the above

22. The memory address register (MAR) is
(a) A general purpose register that hold operands of instructions
(b) A stack pointer
(c) A special registers points to (holds the address
of) the memory location that will be read or written to
(d) A register that holds the instruction that is being executed

23. Consider a virtual memory system that can address a total of 2^{50} bytes. You have unlimited hard drive space, but are limited to 2 GB of semiconductor (physical) memory. Assume that virtual and physical pages

are each 4 KB in size. What is the maximum number of virtual pages in the system?
(a) 31 bits
(b) 38 bits
(c) 19 bits
(d) None of These

24. A recently executed instruction is likely to be executed again very soon is
(a) spatial locality.
(b) temporal locality.
(c) branch prediction.
(d) compiler optimization.

25. A memory system uses the Least Recently Used (LRU) replacement policy for a 4-block cache. If the following sequence of blocks was requested, A B C D E F D A C D, what are the blocks that eventually found in chache
(a) F, D, A, C
(b) D, A, C, D
(c) E, F, A, C
(d) E, F, A, D

26. A processor uses 44-bit virtual addresses with 4 KB pages. Which bits in the virtual address correspond to the "virtual page number" field?
(a) The most significant 34 bits
(b) The least significant 32 bits
(c) The most significant 32 bits
(d) The least significant 12 bits

27. MIPS-32 has.....word size
(a) 16-bit
(b) 32-bit
(c) 64-bit
(d) None of These

28. Convert the following MIPS assembly code into machine language sub$t1, $s7, $s2
(a) 00010000000100001111001111110110
(b) 00010000000100001101111111110110
(c) 00010001100100001111111111110110
(d) 00000010111100100100100000100010

29. In direct addressing mode the operand is given. . . . . in the instruction.
(a) Implicit
(b) Explicit
(c) Not Given
(d) None of these

Questions 30 to 32: A computer system uses 32-bit memory addresses. It has a 128K-byte 8-way set-associative (8 blocks per set) cache, with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.
30. The number of bits in each of the Tag, Set, and Word fields of the memory address
(a) 11, 8, and 6 respectively
(b) 18, 8, and 6 respectively
(c) 15, 9, and 6 respectively
(d) 20, 6, and 8 respectively

31. If direct mapping is used, the number of bits in each of Tag, block, and Word fields of the memory address
(a) 18, 8, and 6 respectively
(b) 15, 8, and 7 respectively
(c) 15, 9, and 6 respectively
(d) 24, 9, and 6 respectively

32. If fully associative mapping is used, the number of bits in each of Tag and Word fields of the memory address
(a) 26 and 6 respectively
(b) 11 and 6 respectively
(c) 32 and 6 respectively
(d) 32 and 0 respectively

33. If multiplexers are used to construct a common bus system for 6 registers of 32 bit each. How many MUX do you need?
(a) twenty
(b) six
(c) thirty two
(d) none is correct

34. Consider a 128 M x 128 memory. How many address bits are needed to access the memory?
(a) 23
(b) 30
(c) 40
(d) 27

Question 2 (6 pts): True or False

1. A page table acts as a cache for the Translation Lookaside Buffer (TLB).

2. A write-through cache need a "dirty" bit for each cache line.

3. A write-back cache typically requires more reads to the main memory than a write-through cache.

4. The main purpose of using larger cache block sizes is to reduce the cache access time.

5. SRAM is more expensive on a cost-per-bit basis as compared to DRAM.

6. A "word" is the natural unit of organization of memory. Different computers may have different word lengths (in bits).

Question 3 (30 pts)

1) Define each of the following:**[04 Marks]**
*(i)*Cache, *(ii)* Virtual Memory, *(iii)*Hit Rate, *(iv)* Miss Rate

2) Show the main difference between temporal and spatial locality? **[02 Marks]**

3) Program to calculate Absolute value of difference between **[10 Marks]**
2 input numbers: |A - B| where:
Program reads A from 4 bytes of memory starting at address 12345670_{16}.
Program reads B from 4 bytes of memory starting at address 12345674_{16}.
Program writes |A-B| to4 bytes of memory starting at address 12345678_{16}.

4) Implement the following C code with MIPS assembly language. **[14 Marks]**

```
// C code
void setArray(int num) {
int i;
int array[10];
for (i = 0; i < 10; i = i + 1) {
array[i] = compare(num, i);
}
}
int compare(int a, int b) {
if (sub(a, b) >= 0)
return 1;
else
return 0;
}
int sub(int a, int b) {
return a – b;
}
```

Mnemonics	Code
Add	32
Sub	34
Addi	8
$s0	16
$s1	17
$s2	18
$s7	23
$t0	8
$t1	9
$t3	11
$t5	13

Good Luck all,
Dr. Nada M. Elshennawy

Tanta University | Department: Elec. Power and Machines Engineering | Faculty of Engineering

Total Marks: 90 Marks

Course Title: Electrical Measurements	Course Code: EPM1202	Year: First year
Date: 16/6/ 2019 (Second term)	Allowed time: 3 hrs	No. of Pages: (2)

الامتحان مكون من 4 أسئلة ويقع في ورقة واحدة في صفحتين

Answer the following questions

Problem number (1) (24 Marks)

a) Chose the BEST answer: **(5 points)**

i. The smallest change in measured value to which the instrument will respond, is known as: a) Precision b) Resolution c) Sensitivity d) Error

ii. The ratio of input signal of a certain instrument its output value, is known as:
a) Precision b) Error c) Resolution d) Sensitivity

iii. A 150 V voltmeter has a guaranteed accuracy of 1 percent at full scale reading. The voltage measured by this instrument is 83 V. The limiting error in percent is:
a) 1.807% b) 1.811% c) 1.829% d) 1.831%

iv. Accuracy of a measurement is an indication of
a) How close the reading is to the average value
b) How close the reading is to nominal value
c) How close the reading is to conventional value
d) How close the reading is to the true value

v. Systematic errors in a certain measuring instrument can be eliminated by
a) Repeating the measurement
b) Changing the measuring instrument
c) Recalibrating the equipment
d) Using correction of zero

b) State if the following sentences are true or false: **(5 points)**

i. Accuracy of a measurement is an indication of total errors in the measurement

ii. Precision of a measurement is an indication of how close the reading is to the average value

iii. Arithmetic error is a type of measurement error in measuring instruments

iv. Percent limiting error is constant with varying the measured value

v. The insertion of an ammeter in a circuit increases the overall resistance, reduces the flowing current and increases the measured current

c) **Design** a multi-range DC ammeter with ranges: 20 mA, 500 mA, 1.0 A and 5.0 A. A PMMC is used with an internal resistance Rm = 5 Ω and a full-scale deflection current I_{fs}= 20 mA. **Calculate** the values of the required shunt resistors and **draw** the complete circuit diagram. Comment on the results. **(7 points)**

d) Derive the equations of a four-section Ayrton shunt. Design an Ayrton shunt ammeter for measuring currents of 50 mA, 500 mA, 3 A and 10 A. The movement has an internal resistance of 50 Ω and a full-scale deflection current of 5 mA. **(7 points)**

Problem number (2) (24 Marks)

a) A basic meter with an internal resistance of 180 Ω and a full-scale deflection current of 100 mA is used in a simple DC ammeter. The ammeter is connected into a certain circuit and gives a reading of 3.5 A on a 5 A range. The reading is checked by a recently calibrated DC ammeter that gives a reading of 4.1 A. The original ammeter has wrong shunt resistance that causes the error. Calculate: **(6 points)**

(i) The value of the faulty shunt.

(ii) The correct shunt for 5 mA range

b) A series type ohmmeter has an internal resistance of 100 Ω and a full-scale deflection current of 1.0 mA. The internal battery has an output voltage of 9 V. The half scale deflection occurs when $R_h = 5000\ \Omega$. **Calculate:** **(6 points)**

i. Values of R_1 and R_2.
ii. Maximum value of R_2 to compensate a 5% drop in battery voltage.
iii. Scale error at a half-scale mark (5000 Ω) when R_2 is set as in (ii).

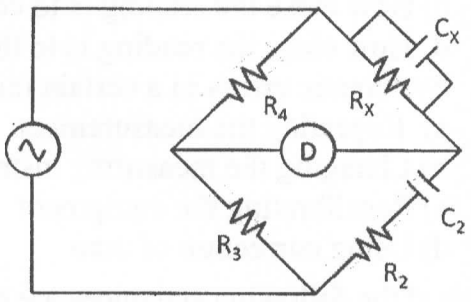
c) Aided with neat sketches, discuss the operation principles of the moving-coil rectifier instruments. **(6 points)**

d) **ONLY with neat sketches**, show how to use electrodynamic instruments as ammeters, voltmeters and Wattmeters. **(6 points)**

Problem number (3) (24 Marks)

a) Explain, with the aid of figure(s) and all necessary equation(s), a bridge for measuring a few Ohm resistance considering the effect of leads resistances. How to compensate for the stray resistances? **(6 points)**

b) The AC bridge shown in the figure is used to measure the capacitance C_X and resistance R_X. (a) Derive the balance equations of the bridge. (b) Given $R_3 = R_4$, $C_2 = 0.2\ \mu F$, $R_2 = 2.5\ k\Omega$ and the frequency of the supply is 1 kHz, determine the values of R_X and C_X at balance. **(8 points)**



c) Explain, with the aid of figures and all necessary equations, how the potentiometer (or the voltage divider variable resistance transducer) is used to measure a mechanical force? Then prove that the potentiometer can be used to indicate the velocity and acceleration of the slide position. **(6 points)**

d) Write down principle of operation of Piezoelectric transducers. How it could be used as Ultrasonic transducers? **(4 points)**

Good Luck

Course Examination Committee

Prof. Ahmed Refaat Azmy Dr. Abd-Elsalam Ahmed

TANTA UNIVERSITY

Electrical Power and Machines Department

Faculty of Engineering

Final EXAM 2018/2019- Second Term

Course	Electrical Circuits (2) (EPM1203)	Time Allowed	3 hours
Students	1st Year (Electrical)	Total Marks	85
Date	June 20th, 2019	Number of pages	3

قبل أن تبدأ إجابتك الرجاء قراءة التعليمات العامة الآتية والالتزام بها بكل دقة:	
١. اكتب رقم السؤال بوضوح.	٢. استخدم الرسومات التوضيحية ذات البيانات الواضحة والكاملة كلما أمكن.
٣. أجب بوضوح سواء باللغة الإنجليزية أو العربية.	٤. لا يشترط الإجابة بترتيب الأسئلة في ورقة الامتحان.
٥. افترض قيمًا معقولة لأية بيانات ناقصة.	٦. فيما عدا الرسومات لا تستخدم القلم الرصاص إلا في أضيق الحدود
٧. ابدأ إجابة كل السؤال في بداية صفحة جديدة (إلا إذا تعذر ذلك)	٨. تجنب تمامًا في إجاباتك استخدام: • اللونين الأحمر والأخضر • سائل التصحيح corrector

Answer ALL the following Six questions and problems:

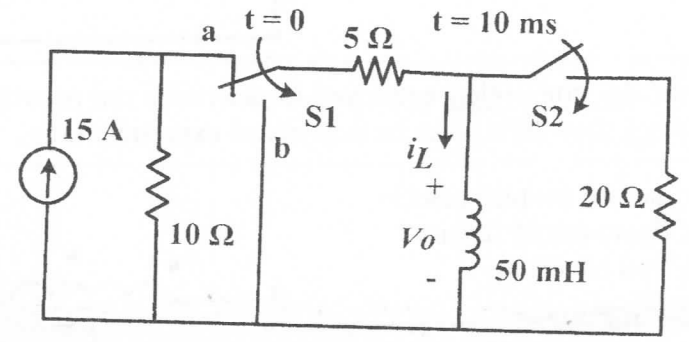
The Third Question (20 marks)

1. For balanced three-phase systems, use **phasor diagrams** to derive the relationship (both magnitude and angle) between the following pairs:
   A) phase and line **voltages** for a positive sequence when system is **star**-connected **(3 marks)**
   B) phase and line **currents** for a negative sequence when system is **delta**-connected. **(3 marks)**
2. **Prove** that neutral line current of a balanced three-phase positive-sequence star-connected system is zero. **Only** use mathematical trigonometric relations. *Do not use phasor diagrams.* **(3 marks)**
3. For a balanced star-connected *positive-sequence* three phase system, show that instantaneous power is time invariant. **(3 marks)**
4. A balanced Y-connected load having an impedance of $72 + j21\ \Omega$/phase is connected in parallel with a balanced Δ-connected load having an impedance of $150+j\ 0\ \Omega$/phase. The two paralleled loads are fed from a Y-connected positive sequence ideal generator through a transmission line having an impedance of $0+j\ 1\ \Omega$/phase. The magnitude of the line-to-neutral voltage of the Y-load is 7650 V. Assuming phase voltage of load terminal "a" as a reference, calculate: **(8 marks)**
   a) transmission line currents.
   b) phase currents in the Δ -connected load.
   c) phase currents in the Y-connected load.
   d) line and phase voltages at the sending end (at generator terminals).
   e) complex power delivered to each load.
   f) complex power delivered by the generator.

Please Turn Over

The Second Question (15 marks)

1. In the circuit shown in figure, for $t < 0$ the switch S1 was on position "a" and switch S2 was open for a long time. At t=0, S1 moves instantaneously to position "b" while S2 remains open. At t= 10 ms, S2 closes. **(9 marks)**
   a) **Find** and **plot** time response of inductor current for $0 < t < 25$ ms.
   b) How milliseconds after S1 moves to position "b" is the energy stored in the inductor equals 4% of its initial value at t=0?



2. A series RLC circuit is supplied from an ac sinusoidal voltage source of rms value of V_s, angular frequency of ω and phase shift of θ with respect to the time reference. The inductor has an initial current of I_o while the capacitor has an initial voltage of V_o. The supply is switched on at time=0. **(6 Marks)**
   (i) Show with a brief explanation and waveforms the general form of the circuit current. Clarify current components.
   (ii) Suggest a necessary condition to obtain a current of zero transient component.

The Third Question (15 marks)

An RLC **series** circuit with zero initial stored energy has a resistance of 250 Ohm and an inductance of 62.5 mH. The circuit was open for a long time. At time t=200 ms, the circuit is switched to a dc voltage source of 60-V.

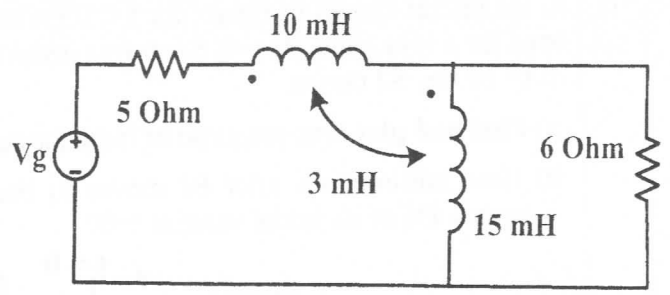
A) Determine the capacitor voltage for the following values of capacitance C:
   1) C= 6.25 μF
   2) C= 2.56 μF
   3) C is adjusted such that the circuit response is critically damped.

B) Sketch *very briefly* (without much calculations and details) the capacitor voltage time response for the three cases of Part A)

Please Turn Over

The Fourth Question (20 marks)

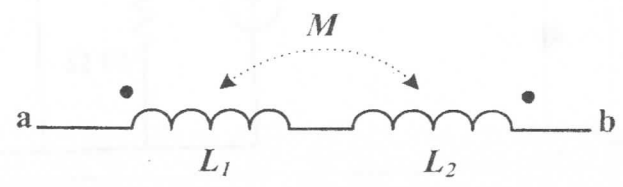
1. For the circuit shown:
   a) Write down the loop equations.
   b) Determine the coefficient of coupling



2. **Explain** the dot convention employed to determine the polarity of the mutually induced voltages. Then show how it can be determined **experimentally**.

3. Show that the two coupled coils in the shown figure can be replaced by a single coil having an inductance of

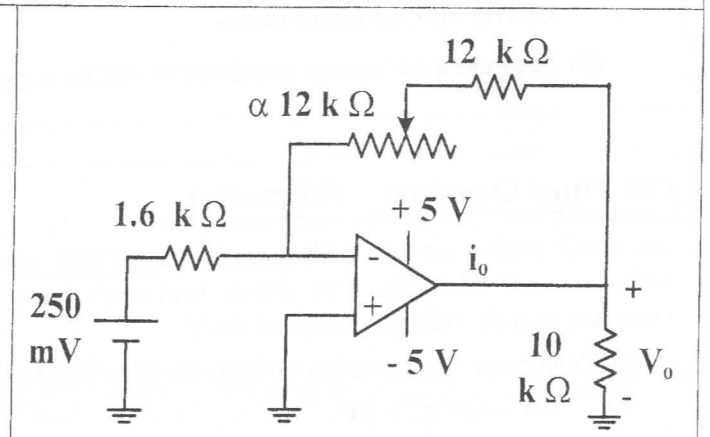
$$L_{ab} = L_1 + L_2 - 2M.$$



The Fifth Question (16 marks)

1. With the aid of a circuit diagram and suitable relations, show how an operational amplifier can be used as an **integrator** .

2. *For the circuit shown*:
   a) Find the range of α for which the omp. amp. does not saturate
   b) Find V_o and i_o when **α =0.272**



3. A single-phase supply is used to feed to a load of 10 Ω resistor connected in series with 10mH reactor. Calculate the RMS value of load current, the total active and reactive power, if the supply voltage is given as:

$$V = 100 \sin 314t + 30 \sin 942t \text{ V}$$

Good Luck and best wishes

Prof. Essam Eddin M. Rashad, Dr. Samir M. Dawoud and exam committee

Tanta University

Department: Engineering Physics and Mathematics
Total Marks: 85 Marks

Faculty of Engineering

Course Title: Engineering Mathematics(2B)
Date: June 2019(2nd term)

Course Code: PME1206
Allowed time: 3 Hrs

Year: 1st Elec,Eng.
No. of Pages: (2)

Q1(21Marks)

(a) Find LT. of

(i) $te^{2t}\sin 3t \cosh t + \delta(t-\pi)\, e^{4t} \sin t$

(ii) $(t^3+t+1)d_{0.3}(t-1) + (t^2+t+4)\, U(t^2-3t+2)$

where, $t \geq 0$, $d_\tau(t-a)$ **is indicator function and** $U(t-a)$ **unit step function**

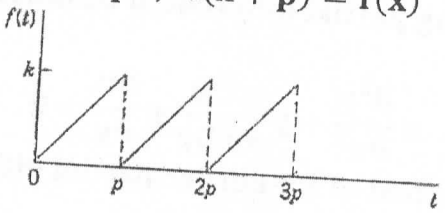
(b) Evaluate

(i) I.L.T of $\frac{e^{-\pi s}}{(s^2+1)(s^2+2)} + 3^{-2s}$

(ii) $\int_5^7 \frac{\sinh tx}{x(x-2)} dx$ **use L.T**

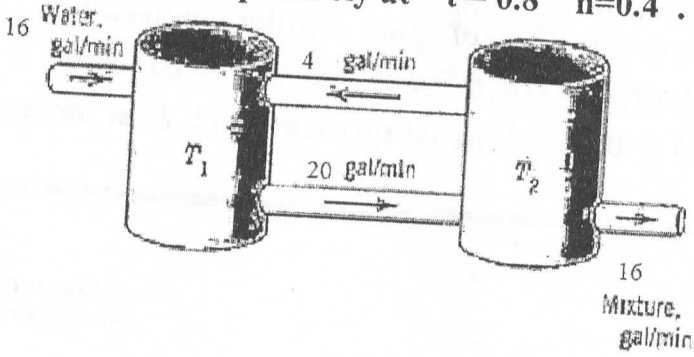
(c) Find Laplace transformation of Saw-tooth wave

$f(x) = \frac{kx}{p}$, $0 \leq x \leq p$, $f(x+p) = f(x)$



Q2(21Marks)

(a) Consider mixture system with tank T_2 contains initially 200 gal of water in which 16 lb of salt are dissolved. Tank T_1 contains initially 100 gal of pure water. Liquid is pumped through the system as indicated, and the mixtures are kept uniform by stirring. Find the amounts of salt $y_1(t)$ and $y_2(t)$ in T_1 and T_2, respectively at $t = 0.8$ h=0.4 .



(b) Find Fourier series of $(x) = x$, $0 \leq x \leq \frac{\pi}{2}$, $f(-x) = -f(x)$, $f(x+\pi) = -f(x)$ **and** $f(x+2\pi) = f(x)$ **then find** $\sum \frac{1}{(2n-1)^2}$, $\sum \frac{(-1)^n}{2n-1}$ **and** $\sum \frac{1}{(2n-1)^4}$

(c) Find Fourier complex for of $f(x) = x^2$ $-\pi \leq x \leq \pi$ **and find Fourier Coefficient** a_0, a_n **and** b_n **from it**

Q3(21Marks)

(a) Show that if f(x+2L) =f(x) , f(x+L) = - f(x) and f(-x) = f(x) then $a_{2n} = 0$

(b) Use Fourier integral form to show that

$$\int_0^{\infty} \frac{\sin\pi\omega \sin x\omega}{1-\omega^2}\, d\omega = \begin{cases} \frac{\pi}{2}\sin x & 0 \le x \le \pi \\ 0 & \pi < x < \infty \end{cases}$$

(c) Deduce Fourier complex form from trigonometric Fourier form

Q4(22Marks)

(a) Transform the following partial differential equation to standard form and solve it

$$x\frac{\partial^2 u}{\partial x^2} + y\frac{\partial^2 u}{\partial x \partial y} + \frac{\partial u}{\partial x} = 0$$

(b) Use characteristic method of first order partial differential equation to solve

$$e^{2x}\frac{\partial u}{\partial x} + 3\frac{\partial u}{\partial y} - 2u = 6x^2$$

with initial condition $u(x,0) = \cosh x$

(c) Consider bar of length L=10 cm, constant cross sectional area $A = 1\ cm^2$ density $\rho = 10.6\ gm/cm^3$, thermal conductivity $K = 1.04\ cal/\ cmsec^0\ c$ and specific heat $\sigma = 0.056\ cal/\ gmc$. Initial temperature $u(x,0) = sin(0.1\pi x) + \frac{1}{2}sin(0.2\pi x)$, $0 \le x \le 10$, and $u(0,t) = u(10,t) = 0$. Find the temperature $u(x,t)$ at any position x and any time t

With Best Wishes

Course Examinatione and Coordinators
Dr. Mohamed Shokry

Tanta University

Department: Electronics & Comm. Engineering
Total Marks: 90 Marks

Faculty of Engineering

Course Title: Electronics (2)	Course Code: EEC1202	Year: First Year
Date: June 2019 (Second term)	Allowed time: 3 hrs	No. of Pages: (2)

Remarks: (answer the following questions... assume any missing data... answers should be supported by sketches...etc)

Question number (1) **(20 Marks)**

1 (a): 1. Mark each statement as either True or False and correct false statements:

1. Small signal analysis shows how a circuit appears to its dc source.
   ( ) True ( ) False
2. The channel width of an n channel JFET can be increased by using a constant V_{DS} and increasing the value of V_{GS} ( ) ***True*** ( ) ***False***
3. The channel width of an n channel JFET can be increased by using a constant V_{GS} and increasing the value of V_{DS} ( ) True ( ) False
4. As UJT current increases from the peak current to valley current, the emitter voltage will increase. ( ) True ( ) False
5. In band to band absorption of a semiconductor the photon energy must be smaller than the band gap to allow optical absorption. ( ) True ( ) False
6. UJT can be programmed to turn on at a desired anode to gate voltage level
   ( ) True ( ) False
7. The voltage gain of a common source amplifier is directly proportional to the value of its transconductance. ( ) True ( ) False
8. In the forward blocking region, the SCR is in the off state.
   ( ) True ( ) False
9. To turn the PMOS transistor ON , the V_{GS} should be less than V_{TH} where V_{TH} itself is negative ( ) True ( ) False
10. The basic operating process of the laser diode is the simulated emission
    ( ) True ( ) False

(b) Explain and determine the region of operation of M_1 in each of the circuits shown in Fig.1 ($V_{TH} = 0.4$ V)

(c) For the circuit shown in Fig.2 , If $\lambda = 0.1\ V^{-1}$, $W/L = 20/0.18$, $V_{TH} = 0.4V$, and . $\mu_n C_{ox} = 200\ \mu A/V^2$ .Calculate V_{DS}, r_o , and the transconductance , then draw the small signal model of the circuit .

Question number (2) **(20 Marks)**

(a) For the circuit shown in Fig.3 , determine the maximum allowable value of W/L if M_1 must remain in saturation. Assume $\lambda = 0$ ($V_{TH} = 0.4$ V, $\mu_n C_{ox} = 200 \mu A/V^2$)

(b) A MOSET is biased at a drain current of 0.5 mA. If $\mu_n C_{ox} = 100\ \mu A/V^2$., W/L = 10, and $\lambda = 0.1\ V^{-1}$. Calculate its small signal parameters, and the intrinsic gain

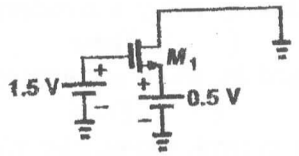
(c) Determine how the transconductance of a MOSFET (operating in saturation) changes if:
(i) W/L is doubled but ID remains constant
(ii) VGS - VTH is doubled but ID remains constant.
(iii) ID is doubled but W/L remains constant

Question number (3) **(15 Marks)**

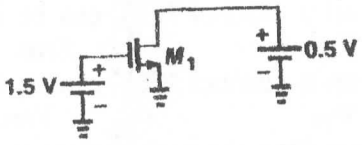
(a) Describe the Light activated silicon controlled rectifier , show how you can use it to energize a latching relay.

(b) *(i)* At what anode voltage V_A will each PUT in Fig.4 (a ,b) begin to conduct

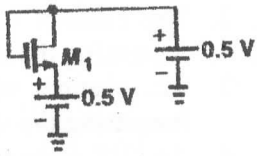
(ii) Draw the current waveform for each circuit when there is a 10V peak sinusoidal voltage at the anode. Neglect the forward voltage of the PUT.



(a)



(b)



(c)

Fig.1

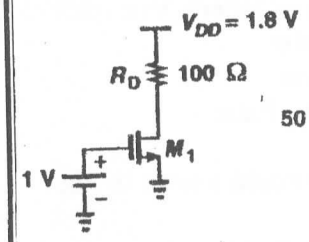


Fig.2

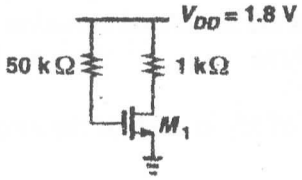


Fig.3

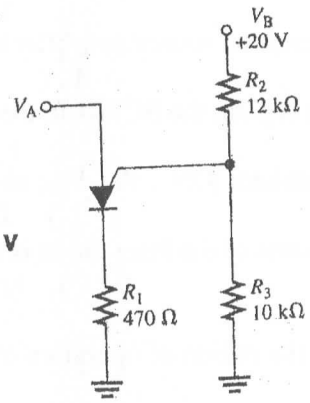
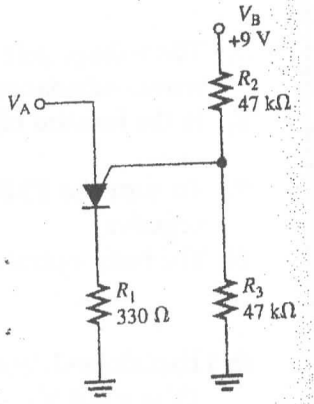


Fig.4 (a)



(b)

Good Luck..... Prof. Mustafa Mahmoud .

Tanta University

Department: Electronics & Electrical Communications

Faculty of Engineering

Total Marks: (36) Marks

Course Title : Electronics2 | Course Code: EEC1202 | Year: 2018/2019

Date: 2 /6/2019 | Allowed time: (80 Min.) | 2nd Term

Part II

Answer the following Questions

Q. 1 : **(12M)**

a) Using diagrams plot optical output vs drive current in case of LED and LASER. diode and hence sketch the corresponding output spectrum .

b)- For the BJT amplifier shown in the Fig.Q1 below :
Determine the critical frequencies associated with the low and high frequency response.
Identify the dominant critical frequency , for gm = 0.52 A/V

Q.2: **(12M)**

a) In the photo-detectors , define the following:
i-Quantum (Shot Noise) . ii- Dark/Leakage Current Noise.

b) An In 0.53 Ga0.47. As photo-diode has the following parameters at a wavelength of 1200 nm: ID = 5 nA , η = 0.90, RL = 900, and the surface leakage current is negligible. The incident optical power is 300 nW (-35dB), and the receiver bandwidth is 18MHz. Find:-
i- The various noise term of the receiver. **ii-** The SNR in decibel

---

Q.3 **(12M)**

a) How the p-n junction PV cell works.

b) Connect a Stack of 36 cells, draw this connection diagram ,however, find the open circuit volt and the actual value at max power.

c) Compare between solar cells versus photodiode with respect to working mode.

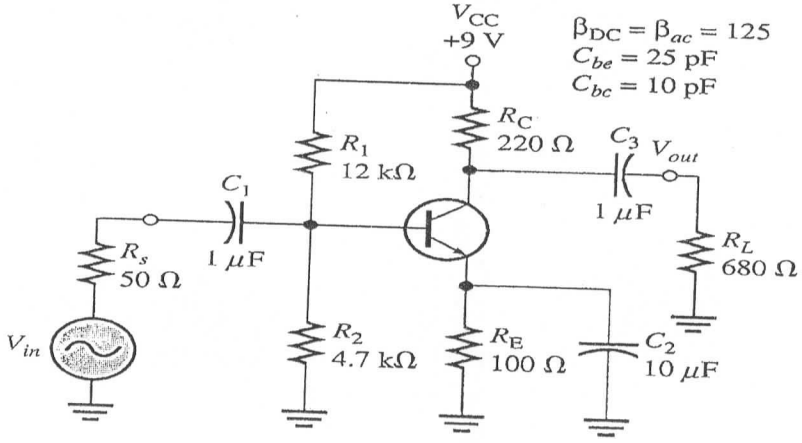


Fig.Q1

N.B : Plank's constant =$(6.625 \times 10^{-34}\ Js)$ - Charge of electron =(1.6×10^{-19}). c
Boltzmann constant =$(1.38 \times 10^{-23}\ J/K)$

Good Luck

Prof. Mohamed El-Said Nasr