B22

Tanta University

Department: Physics and Engineering Mathematics
Total Marks: 85 Marks

Faculty of Engineering

Course Title: Engineering Mathematics 3(a) | Course Code: PME2111 | Year: 2nd
Date: 9/1/ 2023 (First term) | Allowed time: 3 hrs | No. of Pages: (2)

Remarks: (answer the following problems… assume any missing data… answers should be supported by sketches)

Problem number (1) (63 Marks)

a) Find a spline of degree one to interpolate the following data and use the resulting spline to approximate $f(2.2)$

x	1	1.5	2	2.5	3
$y=f(x)$	1	3	7	10	15

b) Using forward, backward, and central methods to estimate the value of $f''(0.5)$ for the function $f(x)=x\cos x$ with $h=0.1$, and hence compare it with the exact value (-1.39764). In addition, find the truncation error for each case.

c) Deduce Trapezoidal Rule $I \cong \frac{h}{2}[f(x)+f(x-h)]$. Use the Composite Trapezoidal Rule with (n=6) to approximate $\int_0^3 x^2 e^x dx$ and find the true Truncation error.

d) Use the Mid-point Runge-Kutta method to obtain an approximation to the solution of the initial value problem (IVP) $\frac{dy}{dx}=(2x-y), x_o=0, y_o=-1$ To get the value of (y) at (x=1) with (n=10) compare the values of the exact solution:
$y(x)=e^{-x}+2x-2$

e) Solve the following B V P:

$y''+(x+1)y'-2y=(1-x^2)e^{-x}, 0\le x\le 1$ With $y_0=-1, y(1)=0$, using the finite difference method with (h = 0.2) compare the results with the exact solution $y=(x-1)e^{-x}$.

f) If $u_t(x,t)=\alpha u_{xx}(x,t)$, $0<x<L$, $0<t<T$ Subject to the boundary conditions:
$u(0,t)=\alpha_0$, $u(L,t)=\beta_0$, $0\le t\le T$
and the initial conditions
$u(x,0)=f(x)$, $0\le x\le L$.
By using finite difference:

$$u_t=\frac{u_i^{j+1}-u_i^j}{k} \quad \text{forward difference}$$

$$u_{xx}=\frac{u_{i+1}^j-2u_i^j+u_{i-1}^j}{h^2} \quad \text{centeral difference}$$

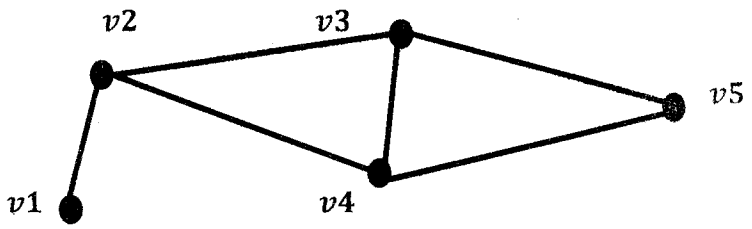
Proof that $u_i^{j+1}=\lambda\left(u_{i+1}^j+u_{i-1}^j\right)+(1-2\lambda)u_i^j$

g) Solve the following PDE $u_t = u_{xx}, 0 \le x \le 1$, with initial condition $u(x,0) = x(1-x)$ and boundary condition $u(0,t) = u(1,t) = 0$ for all $t > 0$ use explicit method with $h = 0.25, \lambda = 0.25$ compute for four times.

Problem number (2) (22 Marks)

a) Use graph vertices counting to find value of 253* 32

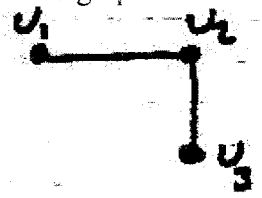
b) From the following graph find connectivity k(G), ε(G), d(G), g(G)and diam(G)



c) Show that, if a graph G=(V,E) is a simple graph, then

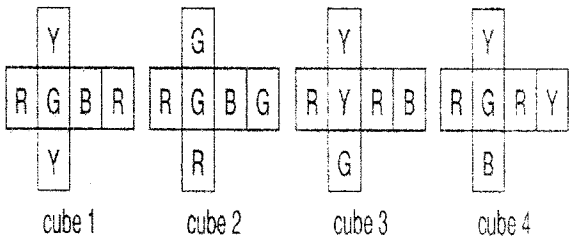
$$|E| \le \binom{V}{2}.$$

d) Use the adjacent matrix to show that the graph is connected



e) Consider isomorphic degree sequence of graph 5,4,3,3,2,2,1,1 use dilation isomorphic theory to find the smallest graphical and graph the obtain every graphs corresponding each steps.

f) Use graph theory concepts to put 4 cubes whose faces are colored red ,blue .green and yellow in 4X1 stack so that all four colors appear on each side of stack



B23

Tanta University | Department: Computer and Automatic Control Engineering | Faculty of Engineering

Total Marks: 75 Marks

Course Title: **Microprocessors and Interfacing Systems**	Course Code: CCE2108	Year: 2nd
Date: 11/01/2023	Allowed Time: 3 hours	**Model B**

Answer ALL the following questions.

Question (1) Choose the correct answer (40 Marks)

1) Which of the following instructions is used to transfers a byte, word, or doubleword of data from an I/O device into the extra segment memory location?
a. INS b. OUTS c. STOS d. LODS

2) The 1 MB byte of memory can be divided into segment
a. 1 Kbyte b. 64 Kbyte c. 33 Kbyte d. 34 Kbyte

3) The 8086 fetches instructions one after another from the _____ segment of memory.
a. CS b. ES c. SS d. IP

4) _____ are the registers that can be addressed directly by a program.
a. Program visible registers b. Program invisible registers
c. Segment registers d. None of the above

5) In Intel 8086 microprocessor ALE signal is made high to
a. Enable the data bus to be used as low order address bus
b. To latch data D0-D7 from data bus
c. To disable data bus
d. To achieve all the functions listed above

6) Intel 8086/8088 microprocessor address bus can locate
a. 1024 locations b. 524,288 locations
c. 1,048,576 locations d. 2,097,152 locations

7) In max mode, control bus signal So,S1 and S2 are sent out in ..... form.
a. encoded b. decoded c. shared d. unshared

8) In 8086 microprocessor one of the following statements is **not true**.
a. Coprocessor is interfaced in MAX mode.
b. I/O can be interfaced in MAX/MIN mode.
c. Coprocessor is interfaced in MIN mode.
d. Memory can be interfaced in MAX/MIN mode.

9) Which of the following instructions modifies the contents of the sign, zero, carry, auxiliary carry, parity, and overflow flags?
a. MOV b. JMP c. ADD d. INS

10) Which of the following components should be connected to the Microprocessor to be able to connect its output pin to more than 10 loads?
a. Latch b. Multiplexer c. Buffer d. Decoder

11) If the clock of 8086/8088 is operated at 8 MHz, how long is one bus cycle?
a. 500 ns b. 800 ns c. 1200 ns d. 200 ns

12) Number of the times the instruction sequence below will loop before coming out of loop is:

```
        MOV CL, 02h
Again:  INC CL
        JNZ Again
```

a. 0 b. 1 c. 255 d. 256 e. 254

13) Which of the following instruction **is not** valid?
a. MOV DS, AX b. MOV AX, 5000H
c. MOV DS, 2000H d. PUSH AX

Determine the address of the memory locations accessed by the following instructions **(Questions 14, 15, 16, and 17)**, assume real-mode memory addressing.

Suppose that:

EAX		50	10
EBX		30	40
ESI		00	60
EDI		00	30
ESP		00	10

CS	**0100**
DS	**0200**
SS	**0300**
EX	**0400**

[Note: ARRAY = 3000H]

14) MOV AX, [BX]
a. 4020 H
b. 5040 H
c. 4040 H, 4041 H
d. 4040 H
e. 5040 H, 5041 H

15) MOV AX, ARRAY[DI]
a. 5000 H, 5001 H
b. 5030 H, 5031 H
c. 4030 H, 4031 H
d. 5030 H

16) PUSH AL
a. 200F H
b. 3011 H
c. 300F H
d. 2010 H, 2011 H
e. 3010 H, 3011 H

17) MOV EAX, [BX + SI + 300H]

a. 5360 H, 5361 H
b. 53A0 H, 53A1 H, 53A2 H, 53A3 H
c. 5360 H, 5361 H, 5362 H, 5363 H
d. 53A0 H, 53A1 H

---

18) During ....., the processors issue the RD or WR signal.

a. T1 b. T2 c. T3 d. T4

19) Intel 8086 microprocessor, READY signal used

a. To indicate to user that the microprocessor is working and is ready for use.
b. To provide proper WAIT states when the microprocessor is communicating with a slow peripheral device.
c. To slow down a fast peripheral device so as to communicate at the microprocessor's device.
d. None of the above.

20) Which of the following is a special software interrupt designed to function as a breakpoint?

a. INT b. INT 3 c. INTO d. IRET

Question (2) (20 Marks)

A. Illustrate the memory map of a personal computer system. **(3 Marks)**

B. What is the difference between real-mode memory addressing and protected-mode memory addressing? Explain briefly the operation of each mode. **(5 Marks)**

C. Consider the two registers **EAX** and **EBX** which contain initial values **A526 FE4A**H, and **4C2A 14BE**H respectively. Write the value of **EBX** register after executing each of the following operations **separately**: **(5 Marks)**

a. MOV AL, BL
b. MOV BH, AH
c. MOV BX, AX
d. MOV EBX, EAX
e. INC BX

D. Explain the usage of "Segment Registers" in real-mode memory operation. And mention four types of segment registers? **(3 Marks)**

E. "In real-mode memory addressing, segment and offset addressing scheme allows relocation". Explain the previous sentence. **(4 Marks)**

Question (3) (15 Marks)

A. Write an assembly program to sum the following two 32-bit numbers using Intel 8086 Microprocessor: (00F5 21A3) + (01B2 0015) **(4 Marks)**

B. How can you separate address/data from the shared address/data bus (AD0-AD15) in the 8086 Microprocessor when accessing a memory device? Describe with Graphs. **(3 Marks)**

C. Write a 8086 assembly program to perform the following task: **(8 Marks)**

Find the **sum of numbers** in a block of data consists of (14) byte-wide numbers stored at memory starting from memory address AD10H to memory address AD1DH. Store the sum in location B000H.

Best Wishes,
Dr. Amr Elkholy

B 24

Model (A)

Tanta University | **Department:** Computers and Control Eng. | **Faculty of Engineering**

Total Marks: 75 Marks

Academic Year: 2022/2023(First Semester)

Course Title: **Digital Systems** Course Code: **CCE2107** **Second Year Students**

Date:**14-1-2023 (End-of-Semester Exam)** Time Allowed: **3 hours** No. of Pages: (**4**)

Model (A)

Answer all the following questions.

Question (1)

A) Shade the circle of the most appropriate answer in your electronic answer sheet: (55 Points)

1) When designing a synchronous counter with D flip-flops (Inputs: D_A, D_B, and D_C /Outputs: A (least significant bit), B, and C (most significant bit)) that goes through the following binary repeated sequence: 0, 4, 1, 6, 0,… . (Hint: Use Karnaugh map to get the simplest form of flip flops input equations); unused states are considered as don't care conditions. If the counter goes to the state 001, the next state will be:
   a) 010 b) 100 c) 000 d) 110 e) None of these
2) Consider the counter in (**point 1**), if the counter goes to the state 110, the next state will be:
   a) 010 b) 100 c) 000 d) 011 e) None of these
3) Consider the counter in **(point 1)**, the input of the first flip-flop A is
   a) $D_A=\overline{A}.C$ b) $D_A=B$ c) $D_A=\overline{B}.C$ d) $D_A=C$ e) None of these
4) Consider the counter in **(point 1)**, the input of the second flip-flop B is
   a) $D_B=A.C$ b) $D_B=\overline{C}$ c) $D_B=\overline{A}.C$ d) $D_B=C$ e) None of these
5) Consider the counter in **(point 1)**, the input of the third flip-flop C is
   a) $D_C=A.\overline{B}$ b) $D_C=A$ c) $D_C=\overline{C}$ d) $D_C=B.C$ e) None of these
6) Consider the counter in (**point 1**), If the counter goes to the state 111, the next state will be:
   a) 010 b) 100 c) 001 d) 000 e) None of these
7) Consider the counter in (**point 1**), If the counter goes to the state 010, the next state will be:
   a) 000 b) 100 c) 001 d) 110 e) None of these
8) Consider the counter in (**point 1**), If the counter goes to the state 011, the next state will be:
   a) 000 b) 100 c) 001 d) 110 e) None of these
9) Consider the counter in (**point 1**), If the counter goes to the state 101, the next state will be:
   a) 010 b) 110 c) 011 d) 111 e) None of these
10) Consider the counter in (**point 1**), The number of stuck states is:
   a) Zero b) 1 c) 2 d) 3 e) None of these
11) Consider the counter in (**point 1**), The number of unused states is:
   a) 2 b) 3 c) 4 d) 5 e) None of these
12) Consider the counter in (**point 1**), the result of connecting all unused states to the 000 state is that usually, this solution leads to complicated Boolean expressions and logic systems.
   a) true b) false c) None of these

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13) Synchronous counters eliminate the delay problems encountered with asynchronous counters because the:
   a) input clock pulses are applied only to the first and last stages
   b) input clock pulses are applied only to the last stage
   c) input clock pulses are not used to activate any of the counter stages
   d) input clock pulses are applied simultaneously to each stage
14) Which of the following is an invalid output state for the BCD counter?
   a) 1110 b) 0000 c) 0010 d) 0001 e) None of these

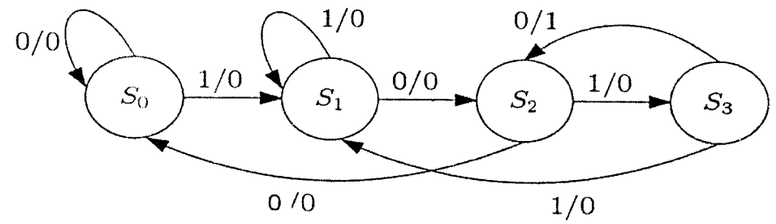
Model (A)

Taking into consideration the following state table, solve the questions from (**point 15**) to (**point 25**), find the unknown values (G1, G2, …….. and G10) in the state table to design a mealy machine sequence detector using five states (A, B, C, D, E), respectively and the initial state is A. Which will detect the sequence 11011 with overlapping includes at maximum. Your detector should output Z a 1 each time the sequence 11011 comes in. The input X is a clocked serial bit stream.

Present State	Next State X=0	Next State X=1	Output Z X=0	Output Z X=1
A	G1	G6	0	0
B	G2	G7	0	0
C	G3	G8	0	0
D	G4	G9	0	0
E	G5	G10	0	1

15) G1=……..
   a) A b) B c) C d)D e) None of these
16) G2=……..
   a) A b) B c) E d)D e) None of these
17) G3=……..
   a) A b) E c) C d)D e) None of these
18) G4=……..
   a) A b) B c) C d)D e) None of these
19) G5=……..
   a) A b) E c) C d)D e) None of these
20) G6=…….. a) A b) B c) C d)E e) None of these
21) G7=…….. a) A b) B c) C d)D e) None of these
22) G8=…….. a) E b) B c) C d)D e) None of these
23) G9=…….. a) A b) B c) C d)E e) None of these
24) G10=…….. a) A b) E c) C d)D e) None of these
25) How many the states required to design a moore machine sequence detector, which will detect the sequence 11011?
   a) 4 b) 5 c) 6 d)7 e) None of these

Taking into consideration the state graph shown in figure, draw tha corresponding algorithmic state machines (ASM) then solve the questions from (point 26) to (point 32)



26) How many state boxes in the corresponding ASM chart?
   a) 8 b) 4 c) 3 d) 6 e) None of these
27) How many decision boxes in the corresponding ASM chart?
   a) 8 b) 5 c) 3 d) 4 e) None of these
28) How many conditional boxes in the corresponding ASM chart?
   a) 8 b) 5 c) 1 d) 9 e) None of these
29) How many blocks in the corresponding ASM chart?
   a) 5 b) 7 c) 4 d) 3 e) None of these
30) How many inputs are required for the control logic part?
   a) 6 b) 4 c) 3 d) 2 e) None of these
31) The control logic part has …….. outputs.
   a) 6 b) 4 c) 3 d) 2 e) None of these
32) What is the minimum number of flip-flops needed to build the control logic part?
   a) 4 b) 3 c) 2 d) 1 e) None of these

33)Pulse stretching is easily accomplished with which type of multivibrator circuit?
a) astable b) monostable c) multistable d) bistable e) None of these

34)An asynchronous 4-bit binary down counter changes from count 2 to count 3. How many transitional states are required?
a) 16 b) 1 c) 2 d) 15 e) None of these

35)What is another name for a bistable multivibrator?
a) a latch b) a flip-flop c) bath a and b are correct d) None of these

36)On the fifth clock pulse, a 4-bit Johnson sequence is Q0 = 0, Q1 = 1, Q2 = 1, and Q3 = 1. On the sixth clock pulse, the sequence is _____.
a) Q0 = 1, Q1 = 0, Q2 = 0, Q3 = 0 b) Q0 = 1, Q1 = 1, Q2 = 1, Q3 = 0
c) Q0 = 0, Q1 = 0, Q2 = 1, Q3 = 1 d) Q0 = 0, Q1 = 0, Q2 = 0, Q3 = 1 e) None of these

37)The bit sequence 0010 is serially entered (right-most bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses?
a) 0000 b) 0010 c) 1000 d) 1111 e) None of these

38)The number of unused states in the 6-bit ring counter is:
a) 6 states b) 12 states c) 58 states d) 24 e) None of these

39)In a 6-bit Johnson counter sequence there are a total of how many states, or bit patterns?
a) 32 b) 6 c) 12 d) 24 e) None of these

40)A modulus-12 ring counter requires a minimum of ..... flip-flops.
a) 3 b) 2 c) 12 d) 4 e) None of these

41)With a 200 kHz clock frequency, eight bits can be serially entered into a shift register in.....
a) 4 µs b) 40 µs c) 20 µs d) 200 ms e) None of these

42)How many clock pulses will be required to completely load serially a 5-bit shift register?
a) 2 b) 3 c) 4 d) 5 e) None of these

43)A MOD-16 ripple up counter is holding the count 1001_2. What will the count be after 31 clock pulses?
a) 1000_2 b) 1010_2 c) 1011_2 d) 1101_2 e) None of these

44)Which is not an example of a truncated modulus?
a) 8 b) 9 c) 11 d) 15 e) None of these

45)Which of the following groups of logic devices would be the minimum required for a MOD-64 synchronous counter?
a) Five flip-flops, four AND gates b) Seven flip-flops, five AND gates
c) Six flip-flops, five AND gates d) Six flip-flops, four AND gates e) None of these

46)Why can a synchronous counter operate at a higher frequency than a ripple counter?
a) The flip-flops change one after the other.
b) The flip-flops change at the same time.
c) A synchronous counter cannot operate at higher frequencies.
d) A ripple counter is faster. e) None of these

47)Consider a flip flop with a setup time of 10 ns and a hold time of 6 ns. The clock input rises at time 40 ns. What it the latest time that the D input can change prior to the clock edge to ensure proper timing?
a) 15 ns b) 20 ns c) 30 ns d) 46 ns e) None of these

48)Consider a flip flop with a setup time of 10 ns and a hold time of 6 ns. The clock input rises at time 40 ns. What it the earliest time that the D input can change after the clock edge to ensure proper timing?
a) 15 ns b) 20 ns c) 30 ns d) 46 ns e) None of these

49)A positive edge-triggered D flip-flop will store a 1 when _____
a) The D input is HIGH and the clock transitions from HIGH to LOW
b) The D input is HIGH and the clock transitions from LOW to HIGH
c) The D input is HIGH and the clock is LOW
d) The D input is HIGH and the clock is HIGH

50) What is one disadvantage of an S-R flip-flop?
a) It has no Enable input b) It has a RACE condition
c) It has no clock input d) Invalid State

51)The K-map simplification for realisation of SR flip-flop from JK flip-flop is .....
a) J=1, K=0 b) J=R, K=S c) J=S, K=R d) J=0, K=1 e) None of these

52)Which one of the following is not the element of the ASM chart?
a) state box b) decision box c) data box d) conditional box

53)A flip flop is an _____
a) Edge sensitive device b) Synchronous device c) Both a and b d)None of these

54)Edge-triggered flip-flops must have:
a) very fast response times. b) at least two inputs to handle rising and falling edges.
c) a pulse transition detector. d) active-LOW inputs and complemented outputs.

55)In VHDL, in which declaration section is a COMPONENT declared?
a) Architecture b) Library c) Entity d) Port map e)None of these

B) Shade the circle in your electronic answer sheet (choose True / False): (20 Marks)

1) To operate correctly, starting a ring shift counter requires clearing all the flip-flops
2) One of the major drawbacks to the use of asynchronous counters is low-frequency applications are limited because of internal propagation delays
3) Once an up-/down-counter begins its count sequence, it cannot be reversed.
4) Moore machine has more states than a Moore machine
5) Moore machine react faster to input
6) In VHDL, it is impossible to use a component twice which was declared only once.
7) In VHDL, complete description of the circuit to be designed is given in Architecture
8) In VHDL, STD_LOGIC data type can have the don't care value
9) In VHDL, libraries can be declared in the declaration part of the architecture
10)In VHDL, internal signals are specified as ports
11)In VHDL, a package consists of commonly used data types and subroutines
12)In VHDL, Bus is a type of signal
13) In VHDL, all signals of a system are defined in the system's entity.
14)In VHDL, ports are signals
15)In VHDL, user cannot define its own integer data type.
16)In VHDL, keywords can be used as identifiers for signals or objects we define
17)In VHDL, to express a number in a base different from the base "10", one uses the following convention: number # base #.
18)In VHDL, to make the readability of large numbers easier, one can insert underscores in the numbers
19)In VHDL, the signal is updated without any delay as soon as the statement is executed.
20)In VHDL, variables must be declared inside a process

End of questions **BEST WISHES**

Course Instructor: Dr. Mohamed Abdalla Attia

B17

Tanta University

Department: Computer Engineering
Total Marks: 100 Marks

Faculty of Engineering

Course Title: Data Structures & Algorithms	Course Code:	Year: 2nd
Date: 1-2023	Allowed time: **3 Hours**	No. of Pages: **(4)**

Model AH044 (NOA = None Of Above)

Complete the following python code that adds a node to the Ordered Linked List:

```
def add(self , item):
    current = ...(1)...
    previous = ...(2)...
    while current ...(3)... :
        if ...(4)... :
            break
        else :
            previous = ...(5)...
            current = ...(6)...
    temp = ...(7)...
    if ...(8)...:
        ...(9)... (self.head)
        ...(10)...
    else :
        ...(9)... ( ...(11)... )
        ...(12)... (...(13)...)
```

1) (1) is:
   a) None b) item c) self.head d) self.tail
2) (2) is:
   a) self.head b) current c) None d) self.tail
3) (3) is:
   a) != None b) = = None c) previous d) NOA
4) (4) is:
   a) Item= =current.getData() b) item>current.getData() c) item<current.getData()
5) (5) is:
   a) current b) self.head c) None d) self.tail
6) (6) is:
   a) previous.getNext() b) current.getNext( ) c) previous.getData() d) NOA
7) (7) is:
   a) None b) BSTNode(item) c) Node(item) d) BSTNode(key)
8) (8) is:
   a) current= = None b) previous= =None c) previous= =current d) NOA
9) (9) is:
   a) temp.setNext b) current.setNext c) previous.setNext d) NOA
10) (10) is:
   a) temp=self.head b) previous=temp c) self.head=temp d) NOA
11) (11) is:
   a) current b) previous c) self.head d) NOA
12) (12) is:
   a) previous.setNext b) current.setNext c) previous.getData d) NOA
13) (13) is:
   a) current b) self.head c) self.tail d) NOA

Complete the following python code that inserts a new item into the BST:

```
def add( self, key, value ) :
    node = self. ...(1)... ( ...(2)... , ...(3)... )
    if node ...(4)... :
        ...(5)...
        return False
    else:
        ...(6)... = self. ...(7)... ( ...(2)... , ...(8)... )
        self.size += 1
        return True
def bstInserT( self, subtree, key, value ) :
    if ...(9)... :
        ...(10)... = ...(11)... ( ...(8)... )
    elif key < ...(12)... :
        ...(13)... = self. ...(14)... ( ...(13)... , ...(8)... )
    else:
        ...(15)... = self. ...(14)... ( ...(15)... , ...(8)... )
    return subtree
```

14) (1) is:
   a) bstMinimum b) bstSearch c) bstInsert d) NOA
15) (2) is:
   a) subtree.left b) self.root c) subtree d) subtree.right
16) (3) is:
   a) self.root b) subtree.right c) key d) root
17) (4) is:
   a) is not None b) is None c) = = None d) NOA
18) (5) is:
   a) self.key=key b) node.key=key c) node.value = value d) NOA
19) (6) is:
   a) subtree.left b) self.root c) subtree.right d) NOA
20) (7) is:
   a) bstDelete b) bstSearch c) bstInsert d) NOA
21) (8) is:
   a) key, value b) key c) value d) NOA
22) (9) is:
   a) subtree is not None b) subtree.right is not None c) subtree is None
23) (10) is:
   a) subtree.left b) subtree.right c) subtree d) key
24) (11) is:
   a) BSTNode b) add c) bstInsert d) NOA
25) (12) is:
   a) subtree.left b) subtree.key c) subtree d) subtree.right
26) (13) is:
   a) subtree.left b) subtree.right c) subtree d) self.subtree
27) (14) is:
   a) bstInsert b) bstDelete c) bstMaximum d) bstInserT
28) (15) is:
   a) subtree.left b) subtree.right c) subtree d) self.subtree

Complete the following python code of smart bubble sort that sorts in ascending order:

```
def smartBubbleSort(alist):
    n = len(alist)
    exchanges = True
    for passnum in range( ...(1)... , 0 , -1 ):
      if exchanges == False:
        ...(2)...
      exchanges=...(3)...
      for i in range(passnum):
        if ...(4)... :
          alist[i] , alist[i+1] = alist[i+1] , alist[i]
          exchanges = True
```

29) (1) is:
a) 2n-1 b) n+1 c) n d) n-1

30) (2) is:
a) alist[i] = alist[i+1] b) break c) return False d) NOA

31) (3) is:
a) False b) True c) exchanges+1 d) NOA

32) (4) is:
a) alist[i+1] != alist[i] b) alist[i+1] > alist[i] c) alist[i+1] < alist[i]

Complete the following function which returns the maximum element of a list:

```
def stringRev(text):
    if len(text) == ...(1)... :
      return ...(2)...
    else:
      return ...(3)... + stringRev( ...(4)... )

print(stringRev( "Hello World!" ) )  # The output is "!dlroW olleH"
```

33) (1) is:
a) 0 b) -1 c) 1 d) 2

34) (2) is:
a) text b) text[1] c) text[-1] d) text[:2]

35) (3) is:
a) text[0] b) text[-1] c) text[1] d) text

36) (4) is:
a) text b) text[0:] c) text[0:-1] d) text[1:]

37) The worst case of BST is ...
a) Tree b) List c) Linked List d) Stack

38) if $T_A(n)=600n$ and $T_B(n)=n^2$, which algorithm is faster for input size 530?
a) A b) B

39) alist[:0] contains ... elements.
a) 3 b) 2 c) 1 d) 0

40) Can you apply BinarySearch algorithm on the Linked List?
a) Yes b) No

Complete the following python code that build a Parse Tree:

```
def buildParseTree(fpexp):
  fplist = fpexp.split()
  pStack = Stack()
  eTree = BinaryTree('')
  pStack.push(...(1)...)
  currentTree = eTree
  for i in fplist:
    if i == '(':
      currentTree. ...(2)...
      pStack. ...(3)...
      currentTree = currentTree.getLeftChild()
    elif i not in '+-*/)':
      currentTree. ...(4)...
      currentTree = ...(5)...
    elif i in '+-*/':
      currentTree. ...(6)...
      currentTree.insertRight('')
      pStack.push(...(7)...)
      ...(8)... = currentTree.getRightChild()
    elif i == ')':
      currentTree = ...(9)...
    else :
      print("error: I don't recognize " + i)
  return ...(10)...
```

41) (1) is:
a) currentTree b) BST c) fpexp d) eTree

42) (2) is:
a) setRootVal(i) b) insertRight('') c) insertLeft('') d) none of the above

43) (3) is:
a) stack.pop( ) b) push(eTree) c) pop( ) d) push(currentTree)

44) (4) is:
a) setRootVal(int(i)) b) insertRight('') c) setRootVal(i) d) insertLeft('')

45) (5) is:
a) currentTree.getRightChild() b) currentTree.getLeftChild()
c) pStack.pop() d) none of the above

46) (6) is:
a) setRootVal(int(i)) b) insertRight('') c) setRootVal(i) d) insertLeft('')

47) (7) is:
a) currentTree b) eTree c) i d) none of the above

48) (8) is:
a) currentTree b) fplist c) i d) none of the above

49) (9) is:
a) Stack.push(eTree) b) Stack.pop( ) c) pStack.pop() d) none of the above

50) (10) is:
a) currentTree b) eTree c) i d) none of the above

B25

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Engineering Department

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Final EXAM 2022/2023 - First Term

Course	Energy conversion (EPM2143)	Time	3 hours
Students	2nd Year (Computer and Control Engineering)	Mark	70
Date	18/01/2023	Number of pages	4

Answer ALL the following questions:

The 1st question (22 Marks Electronic Sheet)

Choose the correct answer and put it in the electronic sheet (ورقة التصحيح الإلكتروني).

1. Centrifugal switch disconnects the auxiliary winding of the single-phase induction motor at about _____ of synchronous speed.
(a) 30 to 40% (b) 70 to 80% (c) 50 to 60% (d) 100%

2. Single phase induction motor of type split-phase usually operates on a power factor of …
(a) 0.6 Lagging (b) 0.85 Lagging (c) 0.85 Leading (d) Unity

3. Torque developed by a single-phase induction motor at starting is …
(a) pulsating (b) rotating (c) uniform (d) zero

4. A shaded pole motor does not have…
(a) Centrifugal switch (b) Capacitor (c) Commutator (d) All the mentioned

5. Which of the following phase sequence represents half-step operation of a VR stepper motor?
(a) A, B, C, A (b) A, C, B, A (c) AB, BC, CA, AB (d) A, AB, B, BC

6. Slip of 3-Phase Induction Motor should always be…
(a) Greater than one (b) Equal to one (c) Less than one (d) Zero

7. A Synchronous Machine having 4 pair-poles and supplied with 60 Hz supply will rotate at.
(a) 900 rpm (b) 1200 rpm (c) 1500 rpm (d) 1800 rpm

8. Synchronous motor.....not varied even applying any load.
(a) frequency (b) speed (c) voltage (d) current

9. If a dc series motor is operated on ac supply, it will have …
(a) excessive sparks (b) poor efficiency (c) poor power factor (d) All the mentioned

10. The speed/load characteristics of a universal motor is same as that of…
(a) A.C. motor (b) D.C. shunt motor (c) D.C. series motor (d) induction motor

11. Armature core of a dc machine is made of …… material
(a) conducting (b) insulating (c) non-magnetic (d) magnetic

12. Laminated yoke in dc motor can reduce …
(a) speed regulation (b) temperature rise (c) iron loss (d) sparking on load

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13. In dc machines, the armature windings are placed on the rotor because of the necessity for …
(a) electromechanical energy conversion
(b) generation of voltage
(c) commutation
(d) development of torque

14. Armature reaction in a dc shunt generator, running at full load with the brushes not shifted from the geometrical neutral plane and saturation neglected, is …
(a) absent (b) demagnetizing (c) cross-magnetizing (d) magnetizing

15. Due to magnetic saturation, the flux per pole in a dc machine without brush shift …
(a) increases in both the generators and the motors with load
(b) decreases in both the generators and the motors with load
(c) increases in generators but decreases in motors with load
(d) decreases in generators and increases in motors with load

16. A dc shunt generator having a shunt field of 50 Ω was generating normally at 1000 rpm. The critical resistance of the machine was 80 Ω. Due to some reasons, the speed of the generator became such that the generator just failed to generate. The speed at that time must have been …
(a) 1600 rpm (b) 800 rpm (c) 625 rpm (d) 500 rpm

17. A dc shunt generator when driven without connecting field winding shows an open-circuit terminal voltage of 12 V. When field winding is connected and excited, the terminal voltage drops to zero because …
(a) critical resistance is higher than field resistance
(b) there is no residual magnetism in the field circuit
(c) field winding has got wrongly connected
(d) none of the above

18. The simplest way of shifting load from one shunt generator to the other operating generator in parallel is by …
(a) changing the speed
(b) changing the armature resistance
(c) changing the field rheostat
(d) using equalizer connection

19. A 400 V dc shunt motor takes 5 A at no load. $R_a = 0.5\ \Omega$, $R_f = 200\ \Omega$. What is the ratio of speed from full load to no load when the dc shunt motor takes 50 A on full load?
(a) 0.94 (b) 0.8 (c) 0.6 (d) 0.4

20. A 240 V dc shunt motor with an armature resistance of 0.5 Ω has a full-load current of 40 A. Find the ratio of the starting torque to the full-load torque when a resistance of 1 Ω is connected in series with the armature …
(a) 4 (b) 12 (c) 6 (d) none of the above

21. For a dc series motor having linear magnetization and negligible armature resistance, the load torque is T. Speed of the motor is …
(a) inversely proportional to $\sqrt{T}$
(b) directly proportional to $\sqrt{T}$
(c) inversely proportional to T^2
(d) directly proportional to T^2

22. Which of the following dc motors has almost constant speed over their full-load range?
(a) Shunt (b) Series (c) Cumulative compound (d) None of these

The 2nd question (12 marks = 4 electronic sheet + 8 Booklet)

A single-phase, 220 V, series motor has the following standstill parameters: Rt = 1 Ω, Lt = 0.05 H. The motor is connected to a 220 V dc supply and rotates at 1400 rpm when loaded to draw a current of 10A. When it is connected to a 220 V ac supply and draws a current of 10A.

Solve the above problem to determine the following then choose the closest answer and put it in the answer sheet (حل المسألة فى كراسة الأجابة أولا ثم أختار الناتج فى ورقة التصحيح الإلكتروني).

23. Motor speed at f = 50Hz
(a) 1500 rpm (b) 480 rpm (c) 960 rpm (d) 750 rpm

24. Motor Power factor at f= 50Hz
(a) 0.6 lag (b) 0.7 lag (c) 0.7 lead (d) 0.6 lead

25. Motor speed at f = 16.67 Hz
(a) 1358 rpm (b) 679 rpm (c) 750 rpm (d) 240 rpm

26. Motor power factor at f = 16.67 Hz
(a) 0.6 lag (b) 0.7 lag (c) 0.97 lead (d) 0.97 lag

The 3rd question (9 marks = 3 electronic sheet + 6 Booklet)

A 3-phase, 20hp, 500V, 50Hz, 6-pole, star connected induction motor running at 950rpm with 0.85 lagging power factor. The mechanical losses are 1hp, the stator copper losses are 1500W, while the core losses are 500W.

Solve the above problem to determine the following then choose the closest answer and put it in the answer sheet (حل المسألة فى كراسة الأجابة أولا ثم أختار الناتج فى ورقة التصحيح الإلكتروني).

27. The rotor copper loss is
(a) 635.5W (b) 412.5W (c) 825W (d) 1000W

28. The line current is
(a) 25A (b) 50A (c) 57.013A (d) 7.47A

29. Motor efficiency is.
(a) 76.96% (b) 81% (c) 87.31% (d) 95%

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The 4th question (15 marks= 5 electronic sheet + 10 Booklet)

A 10-hp 120-V 1000 r/min shunt dc motor has a full-load armature current of 70 A when operating at rated conditions. The armature resistance of the motor is R_a = 0.12 Ω, and the field resistance R_f is 40 Ω. The adjustable resistance in the field circuit may be varied over the range from 0 to 200 Ω and is currently set to 100 Ω. Armature reaction may be ignored in this machine. The magnetization curve for this motor, taken at a speed of 1000 r/min, is given in tabular form below:

E_a (V)	5	78	95	112	118	126	130
I_f (A)	0.00	0.80	1.00	1.28	1.44	2.88	4.00

Solve the above problem to determine the following then choose the closest answer and put it in the answer sheet (حل المسألة فى كراسة الأجابة أولا ثم أختار الناتج فى ورقة التصحيح الإلكتروني).

30. The speed of this motor when it is running at the rated conditions specified above is
(a) 1438 r/min (b) 1000 r/min (c) 1348 r/min (d) 800 r/min

31. The output power from the motor is 10 hp at rated conditions. Then, the output torque of the motor is
(a) 62 N.m (b) 71.2 N.m (c) 88 N.m (d) 100 N.m

32. The efficiency of the motor at full load is
(a) 90.8% (b) 77.8% (c) 87.7% (d) 85%

33. If the motor is now unloaded with no changes in terminal voltage or R_{adj}, the no-load speed of the motor is
(a) 1300 r/min (b) 1450 r/min (c) 1850 r/min (d) 1000 r/min

34. The maximum no-load speed possible in this motor is
(a) 2800 r/min (b) 949 r/min (c) 2372 r/min (d) 1000 r/min

The 5th question (12 marks= 4 electronic sheet + 8 Booklet)

A dc machine (10 kW, 250 V, 1000 r/min) has R_a = 0.2 Ω and R_f = 133 Ω. The machine is self-excited and is driven at 1000 r/min. The data for the magnetization curve are

I_f (A)	0	0.1	0.2	0.3	0.4	0.5	0.75	1.0	1.5	2.0
E_a (V)	10	40	80	120	150	170	200	220	245	263

Solve the above problem to determine the following then choose the closest answer and put it in the answer sheet (حل المسألة فى كراسة الأجابة أولا ثم أختار الناتج فى ورقة التصحيح الإلكتروني).

35. The critical field circuit resistance is
(a) 250 Ω (b) 400 Ω (c) 133 Ω (d) 156 Ω

36. The control resistance in the field circuit to get no-load terminal voltage of 250 V is
(a) 156 Ω (b) 400 Ω (c) 23 Ω (d) 0.2 Ω

37. If the field circuit opens, the generated voltage is
(a) 192 V (b) 5 V (c) 250 V (d) 10 V

38. The short-circuit current of the generator is
(a) 2 A (b) 1250 A (c) 50 A (d) 4 A

Good Luck

Dr. Ahmed Elrefaie *Dr. Mohamed Gamal Hussien*